Winbond Electronics Corp.

8-BIT MICROCONTROLLER

Table of Contents-

1. GENERAL DESCRIPTION

The W79E82X series are an 8-bit Turbo 51 microcontroller which has an in-system programmable Flash EPROM which Flash EPROM can program by ICP (In Circuit Program) or by writer. The instruction set of the W79E82X series are fully compatible with the standard 8052. The W79E82X series contain a **16K/8K/4K/2K/1K** bytes of main Flash EPROM; a **256/128** bytes of RAM; **256/128** bytes NVM Data Flash EPROM; two 8-bit bi-directional, one 2-bit bi-directional and bit-addressable I/O ports; two 16-bit timer/counters; 4-channel multiplexed 10-bit A/D convert; 4-channel 10-bit PWM; two serial ports that include a I2C and an enhanced full duplex serial port. These peripherals are supported by 13 sources four-level interrupt capability. To facilitate programming and verification, the Flash EPROM inside the W79E82X series allow the program memory to be programmed and read electronically. Once the code is confirmed, the user can protect the code for security.

2. FEATURES

- Fully static design 8-bit Turbo 51 CMOS microcontroller up to 20MHz when VDD=4.5V to 5.5V, 12MHz when VDD=2.7V to 5.5V
- **16K/8K/4K/2K/1K** bytes of AP Flash ROM, with ICP and external writer programmable mode.
- **256/128** bytes of on-chip RAM
- **256/128** bytes NVM Data Flash EPROM for customer data storage used and 10K writer cycles
- Instruction-set compatible with MSC-51
- Two 8-bit bi-directional and one 2-bit bi-directional ports
- Two 16-bit timer/counters
- 13 interrupts source with four levels of priority
- One enhanced full duplex serial port with framing error detection and automatic address recognition
- The 4 outputs mode and TTL/Schmitt trigger selectable Port
- Programmable Watchdog Timer
- Four -channel 10-bit PWM (Pulse Width Modulator)
- Four-channel multiplexed with 10-bits A/D convert
- One I2C communication port (Master / Slave)
- Eight keypad interrupt inputs
- Two analog comparators
- Configurable on-chip oscillator
- LED drive capability (20mA) on all port pins
- Low Voltage Detect interrupt and reset
- Development Tools:
  - JTAG ICE(In Circuit Emulation) tool
  - ICP(In Circuit Programming) writer
- Packages:
  - Lead Free (RoHS) DIP 20: W79E825ADG

- Lead Free (RoHS) SOP 20: W79E825ASG
- Lead Free (RoHS) DIP 20: W79E824ADG
- Lead Free (RoHS) SOP 20: W79E824ASG
- Lead Free (RoHS) DIP 20: W79E823ADG
- Lead Free (RoHS) SOP 20: W79E823ASG
- Lead Free (RoHS) DIP 20: W79E822ADG
- Lead Free (RoHS) SOP 20: W79E822ASG
- Lead Free (RoHS) DIP 20: W79E821ADG
- Lead Free (RoHS) SOP 20: W79E821ASG

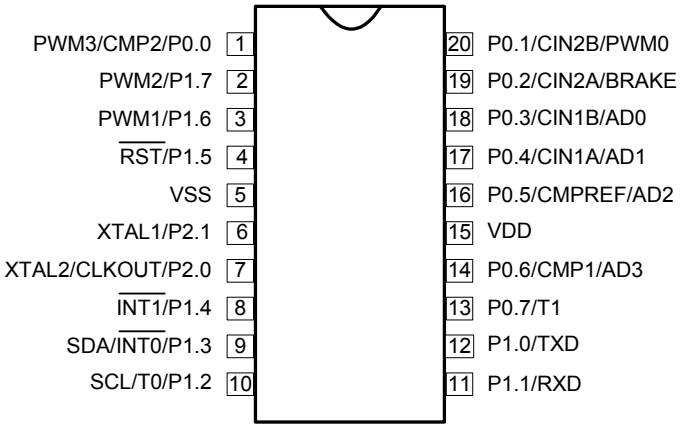
3. PARTS INFORMATION LIST

3.1 Lead Free (RoHS) Parts information list

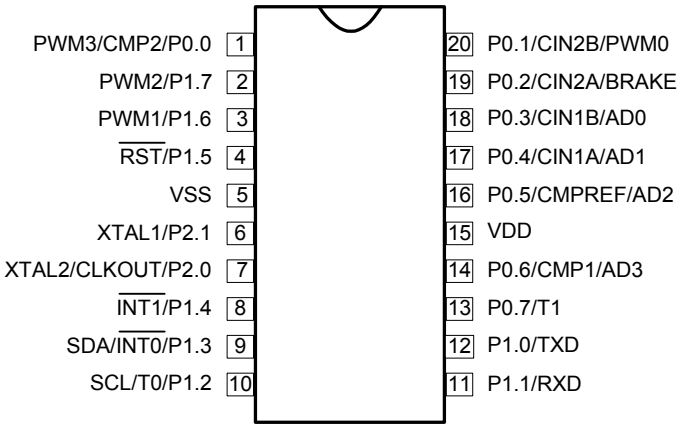
PART NO.	EPROM FLASH SIZE	RAM	NVM FLASH EPROM	ADC	PWM	PACKAGE	REMARK
W79E825ADG	16KB	256B	256B	4x10Bit	4x10Bit	DIP-20 Pin	
W79E825ASG	16KB	256B	256B	4x10Bit	4x10Bit	SOP-20 Pin	
W79E824ADG	8KB	256B	256B	4x10Bit	4x10Bit	DIP-20 Pin	
W79E824ASG	8KB	256B	256B	4x10Bit	4x10Bit	SOP-20 Pin	
W79E823ADG	4KB	128B	128B	4x10Bit	4x10Bit	DIP-20 Pin	
W79E823ASG	4KB	128B	128B	4x10Bit	4x10Bit	SOP-20 Pin	
W79E822ADG	2KB	128B	128B	4x10Bit	4x10Bit	DIP-20 Pin	
W79E822ASG	2KB	128B	128B	4x10Bit	4x10Bit	SOP-20 Pin	
W79E821ADG	1KB	128B	128B	4x10Bit	4x10Bit	DIP-20 Pin	
W79E821ASG	1KB	128B	128B	4x10Bit	4x10Bit	SOP-20 Pin	

4. PIN CONFIGURATION

20 PIN DIP



20 PIN SOP



5. PIN DESCRIPTION

SYMBOL	TYPE	DESCRIPTIONS
$\overline{\text{RST}}$ (P1.5)	I	RESET: A low on this pin for two machine cycles while the oscillator is running resets the device.
XTAL1(P2.1)	I/O	CRYSTAL1: This is the crystal oscillator input. This pin may be driven by an external clock or configurable I/O pin.
XTAL2(P2.0)	I/O	CRYSTAL2: This is the crystal oscillator output. It is the inversion of XTAL1 or configurable I/O pin.
VSS	P	GROUND: Ground potential
VDD	P	POWER: SUPPLY: Supply voltage for operation.
P0.0–P0.7	I/O	PORT 0: Port 0 is four mode output pin and two mode input. The P0.3~P0.6 are 4-channel input ports (ADC0-ADC3) for ADC used.
P1.0–P1.7	I/O	PORT 1: Port 1 is four mode output pin and two mode input. The P1.2(SCL) and P1.3(SDA) is only open drain circuit, and P1.5 only input pin.

* **TYPE:** P: power, I: input, O: output, I/O: bi-directional, H: pull-high, L: pull-low, D: open-drain.

6. FUNCTIONAL DESCRIPTION

The W79E82X series architecture consist of a 4T 8051 core controller surrounded by various registers, **16K/8K/4K/2K/1K** bytes Flash EPROM, **256/128** bytes of RAM, **256/128** bytes NVM Data Flash EPROM, three general purpose I/O ports, two timer/counters, one serial port, one I2C serial I/O, 4 channel PWM with 10-bit counter, 4-channel multiplexed with 10-bit ADC analog input, Flash EPROM program by Writer and ICP.

6.1 On-Chip Flash EPROM

The W79E82X series include one **16K/8K/4K/2K/1K** bytes of main Flash EPROM for application program when operating the in-circuit programming features by the Flash EPROM itself which need Writer or ICP program board to program the Flash EPROM. This ICP(In-Circuit Programming) feature makes the job easy and efficient in which the application needs to update firmware frequently. In some applications, the in-circuit programming feature makes it possible that the end-user is able to easily update the system firmware by themselves without opening the chassis.

6.2 I/O Ports

The W79E82X series have two 8-bit and one 2-bit port, up to 18 I/O pins using on-chip oscillator & /RST is input only by reset options. All ports can be used as four outputs mode when it may set by PxM1.y and PxM2.y registers, it has strong pull-ups and pull-downs, and does not need any external pull-ups. Otherwise it can be used as general I/O port as open drain circuit. All ports can be used bi-directional and these are as I/O ports. These ports are not true I/O, but rather are pseudo-I/O ports. This is because these ports have strong pull-downs and weak pull-ups.

6.3 Serial I/O

The W79E82X series have one serial port that is functionally similar to the serial port of the original 8032 family. However the serial port on the W79E82X series can operate in different modes in order to obtain timing similarity as well. The Serial port has the enhanced features of Automatic Address recognition and Frame Error detection.

6.4 Timers

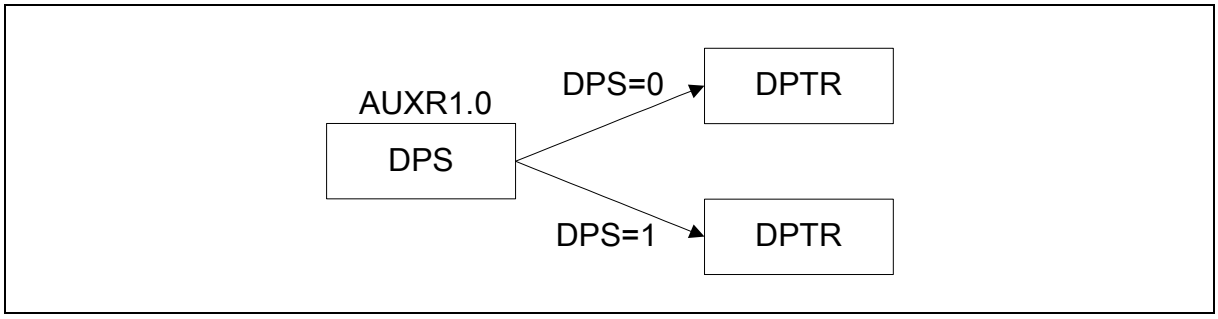
The W79E82X series have two 16-bit timers that are functionally and similar to the timers of the 8052 family. When used as timers, they are set 12 or 4 clocks per count that emulates the timing of the original 8052.

6.5 Interrupts

The Interrupt structure in the W79E82X series is slightly different from that of the standard 8052. Due to the presence of additional features and peripherals, the number of interrupt sources and vectors has been increased.

6.6 Data Pointers

The data pointers of W79E82X series are same as 8052 that has dual 16-bit Data Pointers (DPTR) by setting DPS of AUXR1.0. The figure of dual DPTR is as below diagram.



6.7 Architecture

The W79E82X series are based on the standard 8052 device. It is built around an 8-bit ALU that uses internal registers for temporary storage and control of the peripheral devices. It can execute the standard 8052 instruction set.

6.7.1 ALU

The ALU is the heart of the W79E82X series. It is responsible for the arithmetic and logical functions. It is also used in decision making, in case of jump instructions, and is also used in calculating jump addresses. The user cannot directly use the ALU, but the Instruction Decoder reads the op-code, decodes it, and sequences the data through the ALU and its associated registers to generate the required result. The ALU mainly uses the ACC which is a special function register (SFR) on the chip. Another SFR, namely B register is also used in Multiply and Divide instructions. The ALU generates several status signals which are stored in the Program Status Word register (PSW).

6.7.2 Accumulator

The Accumulator (ACC) is the primary register used in arithmetic, logical and data transfer operations in the W79E82X series. Since the Accumulator is directly accessible by the CPU, most of the high speed instructions make use of the ACC as one argument.

6.7.3 B Register

This is an 8-bit register that is used as the second argument in the MUL and DIV instructions. For all other instructions it can be used simply as a general purpose register.

6.7.4 Program Status Word:

This is an 8-bit SFR that is used to store the status bits of the ALU. It holds the Carry flag, the Auxiliary Carry flag, General purpose flags, the Register Bank Select, the Overflow flag, and the Parity flag.

6.7.5 Scratch-pad RAM

The W79E82X series have a **256/128** bytes on-chip scratch-pad RAM. These can be used by the user for temporary storage during program execution. A certain section of this RAM is bit addressable, and can be directly addressed for this purpose.

6.7.6 Stack Pointer

The W79E82X series have an 8-bit Stack Pointer which points to the top of the Stack. This stack resides in the Scratch Pad RAM in the W79E82X series. Hence the size of the stack is limited by the size of this RAM.

6.8 Power Management

Power Management like the standard 8052, the W79E82X series also have the IDLE and POWER DOWN modes of operation. In the IDLE mode, the clock to the CPU is stopped while the timers, serial ports and interrupt lock continue to operate. In the POWER DOWN mode, all clocks are stopped and the chip operation is completely stopped. This is the lowest power consumption state.

7. MEMORY ORGANIZATION

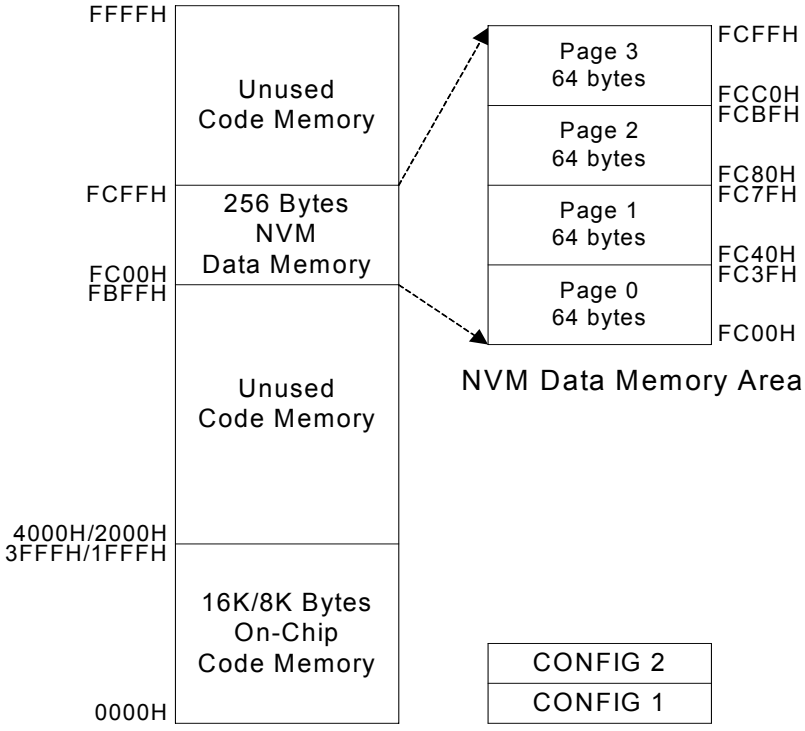
The W79E82X series separate the memory into two separate sections, the Program Memory and the Data Memory. The Program Memory is used to store the instruction op-codes, while the Data Memory is used to store data or for memory mapped devices.

Program Memory

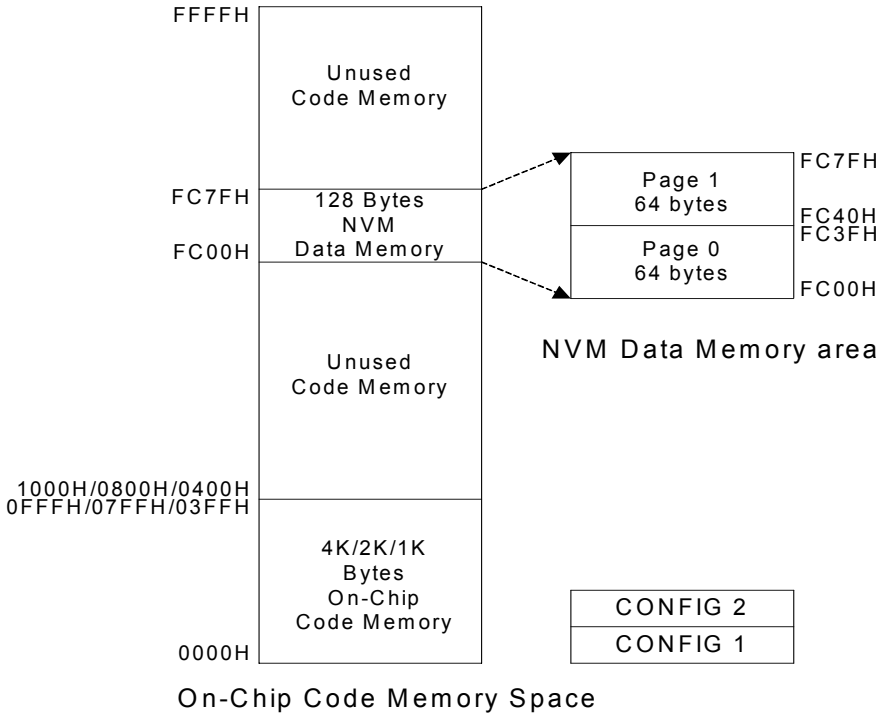
The Program Memory on the W79E82X series can be up to **16K/8K/4K/2K/1K** bytes long. All instructions are fetched for execution from this memory area. The MOVC instruction can also access this memory region.

Data Memory

The NVM Data Memory of Flash EPROM on the W79E82X series can be up to **256/128** bytes long. The W79E82X series read the content of data memory by using "MOVC A,@A+DPTR". To write data is by NVMADDR, NVMDAT and NVMCON SFR's registers.



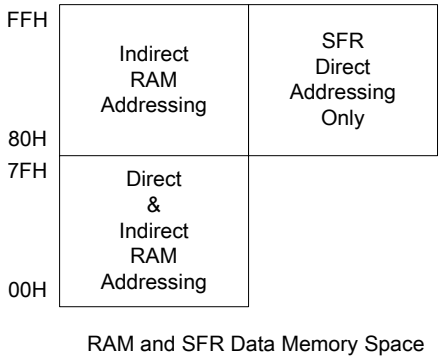
W79E825/W79E824 Memory Map



W79E823/W79E822/W79E821 Memory Map

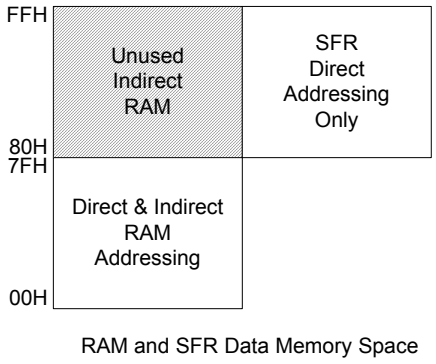
Register Map

As mentioned before the W79E82X series have separate Program and Data Memory areas. The on-chip **256/128** bytes scratch pad RAM is in addition to the external memory. There are also several Special Function Registers (SFRs) which can be accessed by software. The SFRs can be accessed only by direct addressing, while the on-chip RAM can be accessed by either direct or indirect addressing.



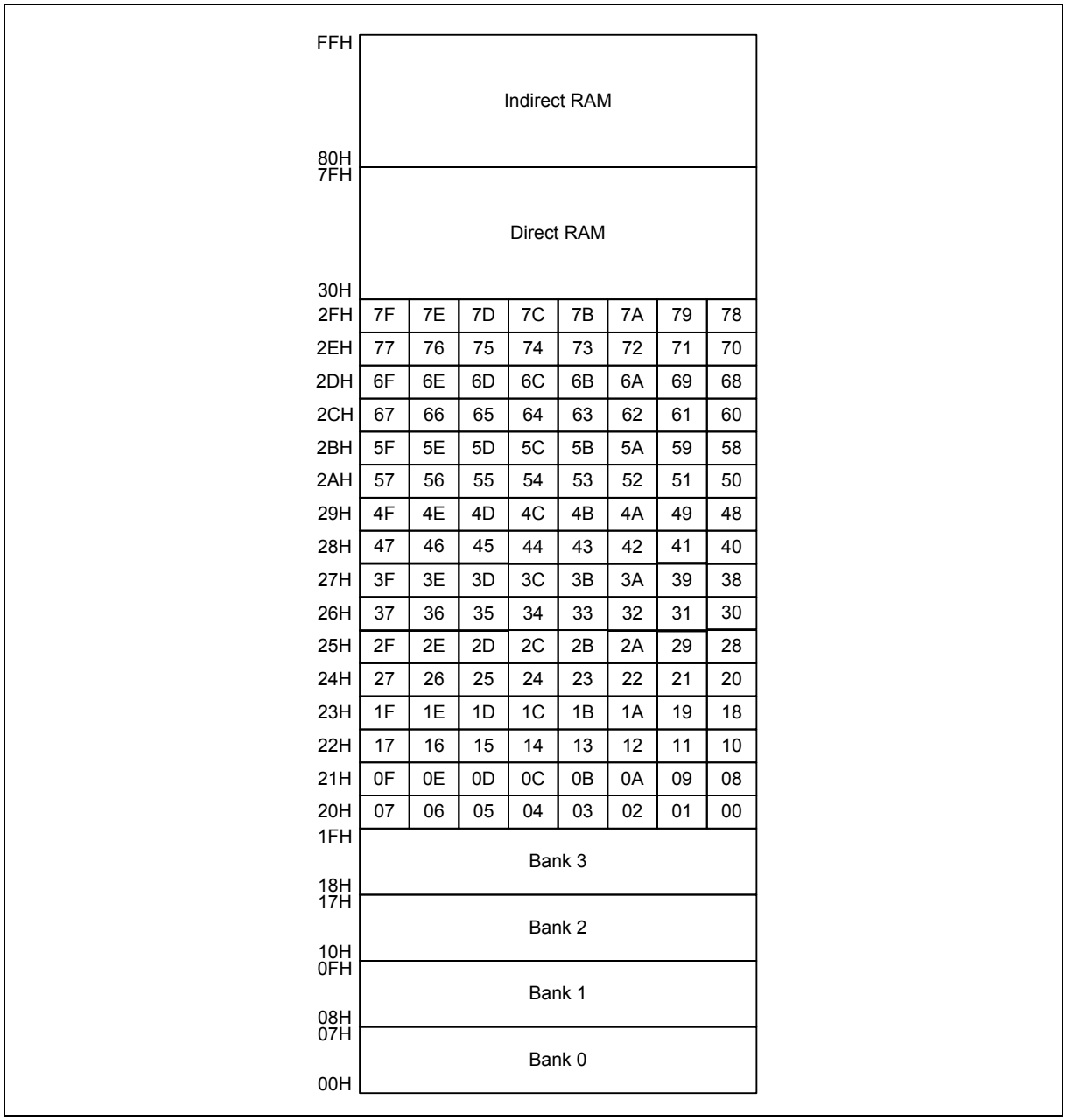
W79E825/W79E824 RAM and SFR Memory Map

The W79E823, W79E822 and W79E821 RAM and SFR memory map as below figure:



W79E823/W79E822/W79E821 RAM and SFR Memory Map

Since the scratch-pad RAM is only **256/128** bytes it can be used only when data contents are small. There are several other special purpose areas within the scratch-pad RAM. These are described as follows.



Working Registers

There are four sets of working registers, each consisting of eight 8-bit registers. These are termed ads Banks 0, 1, 2, and 3. Individual registers within these banks can be directly accessed by separate instructions. These individual registers are named as R0, R1, R2, R3, R4, R5, R6 and R7. However, at one time the W79E82X series can work with only one particular bank. The bank selection is done by setting RS1-RS0 bits in the PSW. The R0 and R1 registers are used to store the address for indirect accessing.

Bit addressable Locations

The Scratch-pad RAM area from location 20h to 2Fh is byte as well as bit addressable. This means that a bit in this area can be individually addressed. In addition some of the SFRs are also bit addressable. The instruction decoder is able to distinguish a bit access from a byte access by the type of the instruction itself. In the SFR area, any existing SFR whose address ends in a 0 or 8 is bit addressable.

Stack

The scratch-pad RAM can be used for the stack. This area is selected by the Stack Pointer (SP), which stores the address of the top of the stack. Whenever a jump, call or interrupt is invoked the return address is placed on the stack. There is no restriction as to where the stack can begin in the RAM. By default however, the Stack Pointer contains 07h at reset. The user can then change this to any value desired. The SP will point to the last used value. Therefore, the SP will be incremented and then address saved onto the stack. Conversely, while popping from the stack the contents will be read first, then the SP is decreased.

8. SPECIAL FUNCTION REGISTERS

The W79E82X series uses Special Function Registers (SFRs) to control and monitor peripherals and their Modes. The SFRs reside in the register locations 80-FFh and are accessed by direct addressing only. Some of the SFRs are bit addressable. This is very useful in cases where we wish to modify a particular bit without changing the others. The SFRs that are bit addressable are those whose addresses end in 0 or 8. The W79E82X series contain all the SFRs present in the standard 8052. However some additional SFRs are added. In some cases the unused bits in the original 8052, have been given new functions. The list of the SFRs is as follows.

Table 1 Special Function Register Location Table

F8	IP1							
F0	B						P0ID	IP1H
E8	IE1							
E0	ACC	ADCCON	ADCH					
D8	WDCON	PWMPL	PWM0L	PWM1L	PWMCON1	PWM2L	PWM3L	PWMCON2
D0	PSW	PWMPH	PWM0H	PWM1H		PWM2H	PWM3H	PWMCON3
C8							NVMCON	NVMDAT
C0	I2CON	I2ADDR					NVMADDR	TA
B8	IP0	SADEN			I2DAT	I2STATUS	I2CLK	I2TIMER
B0		P0M1	P0M2	P1M1	P1M2	P2M1	P2M2	IP0H
A8	IE	SADDR			CMP1	CMP2		
A0	P2	KBI	AUXR1					
98	SCON	SBUF						
90	P1					DIVM		
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	
80	P0	SP	DPL	DPH				PCON

Note: 1. The SFRs in the column with dark borders are bit-addressable

2. The table is condensed with eight locations per row. Empty locations indicate that these are no registers at these addresses. When a bit or register is not implemented, it will read high.

PORT 0

Bit:	7	6	5	4	3	2	1	0
	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

Mnemonic: P0 Address: 80h

P0.7-0: General purpose Input/Output port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. These alternate functions are described below:

BIT	NAME	FUNCTION
7	P0.7	Timer 1 pin or KBI.7 pin of keypad input.
6	P0.6	CMP1 pin of analog comparator or KBI.6 pin of keypad input.
5	P0.5	CMPREF pin of analog comparator or KBI.5 pin of keypad input.
4	P0.4	CIN1A pin of analog comparator or KBI.4 pin of keypad input.
3	P0.3	CIN1B pin of analog comparator or KBI.3 pin of keypad input.
2	P0.2	BRAKE pin of PWM or CIN2A pin of analog comparator or KBI.2 pin of keypad input.
1	P0.1	PWM0 pin or CIN2B pin of analog comparator or KBI.1 pin of keypad input.
0	P0.0	PWM3 pin or CMP2 pin of analog comparator or KBI.0 pin of keypad input.

Note: The initial value of the port is set by CONFIG1.PRHI bit. The default setting for CONFIG1.PRHI =1 which the alternative function output is turned on upon reset. If CONFIG1.PRHI is set to 0, the user has to write a 1 to port SFR to turn on the alternative function output.

STACK POINTER

Bit:	7	6	5	4	3	2	1	0
	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0

Mnemonic: SP Address: 81h

The Stack Pointer stores the Scratchpad RAM address where the stack begins. In other words, it always points to the top of the stack.

DATA POINTER LOW

Bit:	7	6	5	4	3	2	1	0
	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0

Mnemonic: DPL Address: 82h

This is the low byte of the standard 8052 16-bit data pointer.

DATA POINTER HIGH

Bit:	7	6	5	4	3	2	1	0
	DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0

Mnemonic: DPH Address: 83h

This is the high byte of the standard 8052 16-bit data pointer.

This is the high byte of the DPTR 16-bit data pointer.

POWER CONTROL

Bit:	7	6	5	4	3	2	1	0
	SMOD	SMOD0	BOF	POR	GF1	GF0	PD	IDL

Mnemonic: PCON Address: 87h

BIT	NAME	FUNCTION
7	SMOD	1: This bit doubles the serial port baud rate in mode 1, 2, and 3.
6	SMOD0	0: Framing Error Detection Disable. SCON.7 acts as per the standard 8052 function. 1: Framing Error Detection Enable, then and SCON.7 indicates a Frame Error and acts as the FE flag.
5	BOF	0: Cleared by software. 1: Set automatically when a brownout reset or interrupt has occurred. Also set at power on.
4	POR	0: Cleared by software. 1: Set automatically when a power-on reset has occurred.
3	GF1	General purpose user flags.
2	GF0	General purpose user flags.
1	PD	1: the CPU goes into the POWER DOWN mode. In this mode, all the clocks are stopped and program execution is frozen.
0	IDL	1: The CPU goes into the IDLE mode. In this mode, the clocks CPU clock stopped, so program execution is frozen. But the clock to the serial, timer and interrupt blocks is not stopped, and these blocks continue operating.

TIMER CONTROL

Bit:	7	6	5	4	3	2	1	0
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Mnemonic: TCON Address: 88h

BIT	NAME	FUNCTION
7	TF1	Timer 1 overflow flag: This bit is set when Timer 1 overflows. It is cleared automatically when the program does a timer 1 interrupt service routine. Software can also set or clear this bit.
6	TR1	Timer 1 run control: This bit is set or cleared by software to turn timer/counter on or off.
5	TF0	Timer 0 overflow flag: This bit is set when Timer 0 overflows. It is cleared automatically when the program does a timer 0 interrupt service routine. Software can also set or clear this bit.
4	TR0	Timer 0 run control: This bit is set or cleared by software to turn timer/counter on or off.

Continued.

BIT	NAME	FUNCTION
3	IE1	Interrupt 1 Edge Detect: Set by hardware when an edge/level is detected on $\overline{INT1}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the pin.
2	IT1	Interrupt 1 type control: Set/cleared by software to specify falling edge/ low level triggered external inputs.
1	IE0	Interrupt 0 Edge Detect: Set by hardware when an edge/level is detected on $\overline{INT0}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the pin.
0	IT0	Interrupt 0 type control: Set/cleared by software to specify falling edge/ low level triggered external inputs.

TIMER MODE CONTROL

Bit:	7	6	5	4	3	2	1	0
	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0

Mnemonic: TMOD Address: 89h

BIT	NAME	FUNCTION
7	GATE	Gating control: When this bit is set, Timer/counter 1 is enabled only while $\overline{INT1}$ pin is high and TR1 control bit is set. When cleared, Timer 1 is enabled whenever TR1 control bit is set.
6	C/$\overline{T}$	Timer or Counter Select: When cleared, the timer is incremented by internal clocks. When set, the timer counts high-to-low edges of the T1 pin.
5	M1	Timer1 Mode Select bit1: See table below.
4	M0	Timer1 Mode Select bit0: See table below.
3	GATE	Gating control: When this bit is set, Timer/counter 0 is enabled only while $\overline{INT0}$ pin is high and TR0 control bit is set. When cleared, Timer 0 is enabled whenever TR0 control bit is set.
2	C/$\overline{T}$	Timer or Counter Select: When cleared, the timer is incremented by internal clocks. When set, the timer counts high-to-low edges of the T0 pin.
1	M1	Timer0 Mode Select bit1: See table below.
0	M0	Timer0 Mode Select bit0: See table below.

M1, M0: Mode Select bits:

M1	M0	MODE
0	0	Mode 0: 8-bits with 5-bit prescale.
0	1	Mode 1: 16-bits, no prescale.
1	0	Mode 2: 8-bits with auto-reload from THx
1	1	Mode 3: (Timer 0) TL0 is an 8-bit timer/counter controlled by the standard Timer 0 control bits. TH0 is a 8-bit timer only controlled by Timer 1 control bits. (Timer 1) Timer/counter is stopped.

TIMER 0 LSB

Bit:	7	6	5	4	3	2	1	0
	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0

Mnemonic: TL0 Address: 8Ah

TL0.7-0: Timer 0 LSB

TIMER 1 LSB

Bit:	7	6	5	4	3	2	1	0
	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0

Mnemonic: TL1 Address: 8Bh

TL1.7-0: Timer 1 LSB

TIMER 0 MSB

Bit:	7	6	5	4	3	2	1	0
	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0

Mnemonic: TH0 Address: 8Ch

TH0.7-0: Timer 0 MSB

TIMER 1 MSB

Bit:	7	6	5	4	3	2	1	0
	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0

Mnemonic: TH1 Address: 8Dh

TH1.7-0: Timer 1 MSB

Clock Control

Bit:	7	6	5	4	3	2	1	0
	-	-	-	T1M	T0M	-	-	-

Mnemonic: CKCON Address: 8Eh

BIT	NAME	FUNCTION
7~5	-	Reserved
4	T1M	Timer 1 clock select: 0: Timer 1 uses a divide by 12 clocks. 1: Timer 1 uses a divide by 4 clocks.
3	T0M	Timer 0 clock select: 0: Timer 0 uses a divide by 12 clocks. 1: Timer 0 uses a divide by 4 clocks.
2~0	-	Reserved

PORT 1

Bit:	7	6	5	4	3	2	1	0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

Mnemonic: P1 Address: 90h

P1.7-0: General purpose Input/Output port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. These alternate functions are described below:

BIT	NAME	FUNCTION
7	P1.7	PWM 2 Pin
6	P1.6	PWM 1 Pin
5	P1.5	RST Pin or Input Pin by alternative
4	P1.4	INT1 interrupt
3	P1.3	INT0 interrupt or SDA of I^2C
2	P1.2	Timer 0 or SCL of I^2C
1	P1.1	RXD of Serial port
0	P1.0	TXD of Serial port

Divider Clock

Bit:	7	6	5	4	3	2	1	0
	DIVM.7	DIVM.6	DIVM.5	DIVM.4	DIVM.3	DIVM.2	DIVM.1	DIVM.0

Mnemonic: DIVM Address: 95h

The DIVM register is clock divider of uC. Refer OSCILLATOR chapter.

SERIAL PORT CONTROL

Bit:	7	6	5	4	3	2	1	0
	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

Mnemonic: SCON Address: 98h

BIT	NAME	FUNCTION
7	SM0/FE	Serial port mode select bit 0 or Framing Error Flag: The SMOD0 bit in PCON SFR determines whether this bit acts as SM0 or as FE. The operation of SM0 is described below. When used as FE, this bit will be set to indicate an invalid stop bit. This bit must be manually cleared in software to clear the FE condition.
6	SM1	Serial port Mode bit 1: **Mode: SM0 SM1 Description Length Baud rate** 0 0 0 Synchronous 8 4/12 Tclk 1 0 1 Asynchronous 10 Variable 2 1 0 Asynchronous 11 64/32 Tclk 3 1 1 Asynchronous 11 Variable
5	SM2	Multiple processors communication. Setting this bit to 1 enables the multiprocessor communication feature in mode 2 and 3. In mode 2 or 3, if SM2 is set to 1, then RI will not be activated if the received 9th data bit (RB8) is 0. In mode 1, if SM2 = 1, then RI will not be activated if a valid stop bit was not received. In mode 0, the SM2 bit controls the serial port clock. If set to 0, then the serial port runs at a divide by 12 clock of the oscillator. This gives compatibility with the standard 8052. When set to 1, the serial clock become divide by 4 of the oscillator clock. This results in faster synchronous serial communication.
4	REN	Receive enable: When set to 1 serial reception is enabled, otherwise reception is disabled.
3	TB8	This is the 9th bit to be transmitted in modes 2 and 3. This bit is set and cleared by software as desired.
2	RB8	In modes 2 and 3 this is the received 9th data bit. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0 it has no function.
1	TI	Transmit interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in all other modes during serial transmission. This bit must be cleared by software.
0	RI	Receive interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bits time in the other modes during serial reception. However the restrictions of SM2 apply to this bit. This bit can be cleared only by software.

SERIAL DATA BUFFER

Bit:	7	6	5	4	3	2	1	0
	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0

Mnemonic: SBUF Address: 99h

BIT	NAME	FUNCTION
7~0	SBUF	Serial data on the serial port is read from or written to this location. It actually consists of two separate internal 8-bit registers. One is the receive resister, and the other is the transmit buffer. Any read access gets data from the receive data buffer, while write access is to the transmit data buffer.

PORT 2

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	P2.1	P2.0

Mnemonic: P2 Address: A0h

BIT	NAME	FUNCTION
7~2	-	Reserved
1	P2.1	XTAL2 or CLKOUT pin by alternative.
0	P2.0	XTAL1 clock input pin.

Keyboard Interrupt

Bit:	7	6	5	4	3	2	1	0
	KBI.7	KBI.6	KBI.5	KBI.4	KBI.3	KBI.2	KBI.1	KBI.0

Mnemonic: KBI Address: A1h

Keyboard interrupt enable.

BIT	NAME	FUNCTION
7	KBI.7	1: Enable P0.7 as a cause of a Keyboard interrupt.
6	KBI.6	1: Enable P0.6 as a cause of a Keyboard interrupt.
5	KBI.5	1: Enable P0.5 as a cause of a Keyboard interrupt.
4	KBI.4	1: Enable P0.4 as a cause of a Keyboard interrupt.
3	KBI.3	1: Enable P0.3 as a cause of a Keyboard interrupt.
2	KBI.2	1: Enable P0.2 as a cause of a Keyboard interrupt.
1	KBI.1	1: Enable P0.1 as a cause of a Keyboard interrupt.
0	KBI.0	1: Enable P0.0 as a cause of a Keyboard interrupt.

AUX Function Register 1

Bit:	7	6	5	4	3	2	1	0
	KBF	BOD	BOI	LPBOV	SRST	ADCEN	0	DPS

Mnemonic: AUXR1 Address: A2h

BIT	NAME	FUNCTION
7	KBF	Keyboard Interrupt Flag: 1: When any pin of port 0 that is enabled for the Keyboard Interrupt function goes low. Must be cleared by software.
6	BOD	Brown Out Disable: 0: Enable Brownout Detect function. 1: Disable Brownout Detect function and save power.

Continued.

BIT	NAME	FUNCTION
5	BOI	Brown Out Interrupt: 0: Disable Brownout Detect Interrupt function and it will cause chip reset when BOF is set. 1: This prevents Brownout Detection from causing a chip reset and allows the Brownout Detect function to be used as an interrupt.
4	LPBOV	Low Power Brown Out Detect control: 0: When BOD is enable, the Brown Out detect is always turned on by normal run or Power Down mode. 1: When BOD is enable, the 1/16 time will be turned on Brown Out detect circuit by Power Down mode. When uC is in Power Down mode, the BOD will enable internal RC OSC(2MHz~0.5MHZ)
3	SRST	Software reset: 1: reset the chip as if a hardware reset occurred.
2	ADCEN	0: Disable ADC circuit. 1: Enable ADC circuit.
1	0	Reserved
0	DPS	Dual Data Pointer Select 0: To select DPTR of standard 8051. 1: To select DPTR1

INTERRUPT ENABLE

Bit:	7	6	5	4	3	2	1	0
	EA	EADC	EBO	ES	ET1	EX1	ET0	EX0

Mnemonic: IE Address: A8h

BIT	NAME	FUNCTION
7	EA	Global enable. Enable/Disable all interrupts.
6	EADC	Enable ADC interrupt.
5	EBO	Enable Brown Out interrupt.
4	ES	Enable Serial Port interrupt.
3	ET1	Enable Timer 1 interrupt.
2	EX1	Enable external interrupt 1.
1	ET0	Enable Timer 0 interrupt.
0	EX0	Enable external interrupt 0.

SLAVE ADDRESS

Bit:	7	6	5	4	3	2	1	0
	SADDR.7	SADDR.6	SADDR.5	SADDR.4	SADDR.3	SADDR.2	SADDR.1	SADDR.0

Mnemonic: SADDR Address: A9h

BIT	NAME	FUNCTION
7	SADDR	The SADDR should be programmed to the given or broadcast address for serial port 0 to which the slave processor is designated.

Comparator 1 Control Register

Bit:	7	6	5	4	3	2	1	0
	-	-	CE1	CP1	CN1	OE1	CO1	CMF1

Mnemonic: CMP1 Address: Ach

BIT	NAME	FUNCTION
7	-	Reserved
6	-	Reserved
5	CE1	Comparator enable: 0: Disable Comparator. 1: Enabled Comparator. Comparator output need wait stable 10 us after CE1 is first set.
4	CP1	Comparator positive input select: 0: CIN1A is selected as the positive comparator input. 1: CIN1B is selected as the positive comparator input.
3	CN1	Comparator negative input select: 0: The comparator reference pin CMPREF is selected as the negative comparator input. 1: The internal comparator reference Vref is selected as the negative comparator input.
2	OE1	Output enable: 1: The comparator output is connected to the CMP1 pin if the comparator is enabled (CE1 = 1). This output is asynchronous to the CPU clock.
1	CO1	Comparator output: Synchronized to the CPU clock to allow reading by software. Cleared when the comparator is disabled (CE1 = 0).
0	CMF1	Comparator interrupt flag: This bit is set by hardware whenever the comparator output CO1 changes state. This bit will cause a hardware interrupt if enabled and of sufficient priority. Cleared by software and when the comparator is disabled (CE1 = 0).

Comparator 2 Control Register

Bit:	7	6	5	4	3	2	1	0
	-	-	CE2	CP2	CN2	OE2	CO2	CMF2

Mnemonic: CMP2 Address: ADh

BIT	NAME	FUNCTION
7	-	Reserved
6	-	Reserved
5	CE2	Comparator enable: 0: Disable Comparator. 1: Enabled Comparator. Comparator output need wait stable 10 us after CE2 is first set.
4	CP2	Comparator positive input select: 0: CIN2A is selected as the positive comparator input. 1: CIN2B is selected as the positive comparator input.
3	CN2	Comparator negative input select: 0: The comparator reference pin CMPREF is selected as the negative comparator input. 1: The internal comparator reference Vref is selected as the negative comparator input.
2	OE2	Output enable: 1: The comparator output is connected to the CMP2 pin if the comparator is enabled (CE2 = 1). This output is asynchronous to the CPU clock.
1	CO2	Comparator output: Synchronized to the CPU clock to allow reading by software. Cleared when the comparator is disabled (CE2 = 0).
0	CMF2	Comparator interrupt flag: This bit is set by hardware whenever the comparator output CO2 changes state. This bit will cause a hardware interrupt if enabled and of sufficient priority. Cleared by software and when the comparator is disabled (CE2 = 0).

Port 0 Output Mode 1

Bit:	7	6	5	4	3	2	1	0
	P0M1.7	P0M1.6	P0M1.5	P0M1.4	P0M1.3	P0M1.2	P0M1.1	P0M1.0

Mnemonic: P0M1 Address: B1h

Port 0 Output Mode 2

Bit:	7	6	5	4	3	2	1	0
	P0M2.7	P0M2.6	P0M2.5	P0M2.4	P0M2.3	P0M2.2	P0M2.1	P0M2.0

Mnemonic: P0M2 Address: B2h

Port 1 Output Mode 1

Bit:	7	6	5	4	3	2	1	0
	P1M1.7	P1M1.6	-	P1M1.4	-	-	P1M1.1	P1M1.0

Mnemonic: P1M1 Address: B3h

Port 1 Output Mode 2

Bit:	7	6	5	4	3	2	1	0
	P1M2.7	P1M2.6	-	P1M2.4	-	-	P1M2.1	P1M2.0

Mnemonic: P1M2 Address: B4h

Port 2 Output Mode 1

Bit:	7	6	5	4	3	2	1	0
	P2S	P1S	P0S	ENCLK	T1OE	T0OE	P2M1.1	P2M1.0

Mnemonic: P2M1 Address: B5h

BIT	NAME	FUNCTION
7	P2S	1: Enables Schmitt trigger inputs on Port 2.
6	P1S	1: Enables Schmitt trigger inputs on Port 1.
5	P0S	1: Enables Schmitt trigger inputs on Port 0.
4	ENCLK	1: To use the on-chip RC oscillator, a clock output is enabled on the XTAL2 pin (P2.0).
3	T1OE	1: The P0.7 pin is toggled whenever Timer 1 overflows. The output frequency is therefore one half of the Timer 1 overflow rate.
2	T0OE	1: The P1.2 pin is toggled whenever Timer 1 overflows. The output frequency is therefore one half of the Timer 1 overflow rate.
1	P2M1.1	To control the output configuration of P2.1.
0	P2M1.0	To control the output configuration of P2.0.

Port 2 Output Mode 2

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	P2M2.1	P2M2.0

Mnemonic: P2M2 Address: B6h

Port Output Configuration Settings:

PXM1.Y	PXM2.Y	PORT INPUT/OUTPUT MODE
0	0	Quasi-bidirectional
0	1	Push-Pull
1	0	Input Only (High Impedance) P2M1.PxS=0, TTL input P2M1.PxS=1, Schmitt input
1	1	Open Drain

Interrupt High Priority

Bit:	7	6	5	4	3	2	1	0
	-	PADCH	PBOH	PSH	PT1H	PX1H	PT0H	PX0H

Mnemonic: IP0H Address: B7h

BIT	NAME	FUNCTION
7	-	This bit is un-implemented and will read high.
6	PADCH	1: To set interrupt high priority of ADC is highest priority level.
5	PBOH	1: To set interrupt high priority of Brown Out Detector is highest priority level.
4	PSH	1: To set interrupt high priority of Serial port 0 is highest priority level.
3	PT1H	1: To set interrupt high priority of Timer 1 is highest priority level.
2	PX1H	1: To set interrupt high priority of External interrupt 1 is highest priority level.
1	PT0H	1: To set interrupt high priority of Timer 0 is highest priority level.
0	PX0H	1: To set interrupt high priority of External interrupt 0 is highest priority level.

Interrupt Priority0

Bit:	7	6	5	4	3	2	1	0
	-	PADC	PBO	PS	PT1	PX1	PT0	PX0

Mnemonic: IP0 Address: B8h

BIT	NAME	FUNCTION
7	-	This bit is un-implemented and will read high.
6	PADC	1: To set interrupt priority of ADC is higher priority level.
5	PBO	1: To set interrupt priority of Brown Out Detector is higher priority level.
4	PS	1: To set interrupt priority of Serial port 0 is higher priority level.
3	PT1	1: To set interrupt priority of Timer 1 is higher priority level.
2	PX1	1: To set interrupt priority of External interrupt 1 is higher priority level.
1	PT0	1: To set interrupt priority of Timer 0 is higher priority level.
0	PX0	1: To set interrupt priority of External interrupt 0 is higher priority level.

SLAVE ADDRESS MASK ENABLE

Bit:	7	6	5	4	3	2	1	0

Mnemonic: SADEN Address: B9h

BIT	NAME	FUNCTION
7~0	SADEN	This register enables the Automatic Address Recognition feature of the Serial port 0. When a bit in the SADEN is set to 1, the same bit location in SADDR will be compared with the incoming serial data. When SADEN is 0, then the bit becomes a "don't care" in the comparison. This register enables the Automatic Address Recognition feature of the Serial port 0. When all the bits of SADEN are 0, interrupt will occur for any incoming address.

I2C Data Register

Bit:	7	6	5	4	3	2	1	0
	I2DAT.7	I2DAT.6	I2DAT.5	I2DAT.4	I2DAT.3	I2DAT.2	I2DAT.1	I2DAT.0

Mnemonic: I2DAT Address: BCh

BIT	NAME	FUNCTION
0~7	I2DAT	The data register of I2C.

I2C Status Register

Bit:	7	6	5	4	3	2	1	0
						-	-	-

Mnemonic: I2STATUS Address: BDh

BIT	NAME	FUNCTION
0~7	I2STATUS	The status register of I2C: The three least significant bits are always 0. The five most significant bits contain the status code. There are 23 possible status codes. When I2STATUScontains F8H, no serial interrupt is requested. All other I2STATUS values correspond to defined I2C states. When each of these states is entered, a status interrupt is requested (SI = 1). A valid status code is present in I2STATUS one machine cycle after SI is set by hardware and is still present one machine cycle after SI has been reset by software. In addition, states 00H stands for a Bus Error. A Bus Error occurs when a START or STOP condition is present at an illegal position in the formation frame. Example of illegal position are during the serial transfer of an address byte, a data byte or an acknowledge bit.

I2C Baud Rate Control Register

Bit:	7	6	5	4	3	2	1	0
	I2CLK.7	I2CLK.6	I2CLK.5	I2CLK.4	I2CLK.3	I2CLK.2	I2CLK.1	I2CLK.0

Mnemonic: I2CLK Address: BEh

BIT	NAME	FUNCTION
7~ 0	I2CLK	The I2C clock rate bits.

I2C Timer Counter Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	ENTI	DIV4	TIF

Mnemonic: I2TIMER Address: BFh

BIT	NAME	FUNCTION
7~3	-	Reserved.
2	ENTI	Enable I2C 14-bits Timer Counter: 0: Disable 14-bits Timer Counter count. 1: Enable 14-bits Timer Counter count. After enable ENTI and ENSI, the 14-bit counter will be counted. When SI flag of I2C is set, the counter will stop to count and 14-bits Timer Counter will be cleared.
1	DIV4	I2C Timer Counter clock source divide function: 0: The 14-bits Timer Counter source clock is Fosc clock. 1: The 14-bits Timer Counter source clock is divided by 4.
0	TIF	The I2C Timer Counter count flag: 0: The 14-bits Timer Counter is not overflow. 1: The 14-bits Timer Counter is overflow. Before enable I2C Timer(both ENTI, ENSI =[1,1]) the SI must be cleared. If I2C interrupt is enabled then will executed I2C interrupt service routine. This bit is cleared by software.

I2C Control Register

Bit:	7	6	5	4	3	2	1	0
	-	ENS1	STA	STO	SI	AA	-	-

Mnemonic: I2CON Address: C0h

BIT	NAME	FUNCTION
7	-	Reserved.
6	ENS1	Enable I2C serial function.
5	STA	The START flag of I2C.
4	STO	The STOP flag of I2C.
3	SI	The interrupt flag of I2C.
2	AA	The Assert Acknowledge flag of I2C.
1	-	Reserved.
0	-	Reserved.

I2C Address Register

Bit:	7	6	5	4	3	2	1	0
	I2ADDR.7	I2ADDR.6	I2ADDR.5	I2ADDR.4	I2ADDR.3	I2ADDR.2	I2ADDR.1	GC

Mnemonic: I2ADDR Address: C1h

BIT	NAME	FUNCTION
7~1	I2ADDR.7 ~ I2ADDR1	I2C Address register: The 8051 uC can read from and write to this 8-bit, directly addressable SFR. The content of this register is irrelevant when I2C is in master mode. In the slave mode, the seven most significant bits must be loaded with the MCU's own address. The I2C hardware will react if either of the address is matched.
0	GC	General Call Function. 0: Disable General Call Function. 1: Enable General Call Function.

NVN ADDRESS

Bit:	7	6	5	4	3	2	1	0
	NVMADDR.7	NVMADDR.6	NVMADDR.5	NVMADDR.4	NVMADDR.3	NVMADDR.2	NVMADDR.1	NVMADDR.0

Mnemonic: NVMADDR Address: C6h

BIT	NAME	FUNCTION
7~0	NVMADDR.7 ~ NVMADDR.0	The NVM address: The register indicates NVM data memory of low byte address on On-Chip code memory space.

TIMED ACCESS

Bit:	7	6	5	4	3	2	1	0
	TA.7	TA.6	TA.5	TA.4	TA.3	TA.2	TA.1	TA.0

Mnemonic: TA Address: C7h

BIT	NAME	FUNCTION
7~0	TA	The Timed Access register: The Timed Access register controls the access to protected bits. To access protected bits, the user must first write AAH to the TA. This must be immediately followed by a write of 55H to TA. Now a window is opened in the protected bits for three machine cycles, during which the user can write to these bits.

NVM CONTROL

Bit:	7	6	5	4	3	2	1	0
	EER	EWR	-	-	-	-	-	-

Mnemonic: NVMCON Address: CEh

BIT	NAME	FUNCTION
7	EER	NVM page(n) erase bit. 0: Without erase NVM page(n). 1: Set this bit to erase NVM data of page(n) to FFH. The NVM has 4 pages and each page have 64 bytes data memory. Before select page by NVMADDR register that will automatic enable page area, after set this bit, the page will be erased and program counter will halt at this instruction. After finished, program counter will kept next instruction then executed. The NVM page's address define as below table.
6	EWR	NVM data write bit 0: Without write NVM data. 1: Set this bit to write NVM bytes and program counter will halt at this instruction. After write is finished, program counter will kept next instruction then executed.
5~0	-	Reserved

NVM Page(n) Area Definition Table:

PAGE	START ADDRESS	END ADDRESS
0	00H	3FH
1	40H	7FH
2	***80H***	***BFH***
3	***C0H***	***FFH***

Note: The W79E823, W79E822 and W79E821 without page 2 and page 3.

NVM DATA

Bit:	7	6	5	4	3	2	1	0
	NVMDAT.7	NVMDAT.6	NVMDAT.5	NVMDAT.4	NVMDAT.3	NVMDAT.2	NVMDAT.1	NVMDAT.0

Mnemonic: NVMDATA Address: CFh

BIT	NAME	FUNCTION
7~0	NVMDAT.7 ~ NVMDAT.0	The NVM data write register. The read NVM data is by MOVC instruction.

PROGRAM STATUS WORD

Bit:	7	6	5	4	3	2	1	0
	CY	AC	F0	RS1	RS0	OV	F1	P

Mnemonic: PSW Address: D0h

BIT	NAME	FUNCTION
7	CY	Carry flag: Set for an arithmetic operation which results in a carry being generated from the ALU. It is also used as the accumulator for the bit operations.
6	AC	Auxiliary carry: Set when the previous operation resulted in a carry from the high order nibble.

Continued.

BIT	NAME	FUNCTION
5	F0	User flag 0: The General purpose flag that can be set or cleared by the user.
4	RS1	Register bank select bits:
3	RS0	Register bank select bits:
2	OV	Overflow flag: Set when a carry was generated from the seventh bit but not from the 8th bit as a result of the previous operation, or vice-versa.
1	F1	User Flag 1: The General purpose flag that can be set or cleared by the user by software.
0	P	Parity flag: Set/cleared by hardware to indicate odd/even number of 1's in the accumulator.

RS.1-0: Register Bank Selection Bits:

RS1	RS0	REGISTER BANK	ADDRESS
0	0	0	00-07h
0	1	1	08-0Fh
1	0	2	10-17h
1	1	3	18-1Fh

PWM Counter High Bits Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	PWMP.9	PWMP.8

Mnemonic: PWMPH Address: D1h

BIT	NAME	FUNCTION
7~2	-	Reserved
1~0	PWMP.9 ~PWMP.8	The PWM Counter Register bit9~8.

PWM 0 High Bits Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	PWM0.9	PWM0.8

Mnemonic: PWM0H Address: D2h

BIT	NAME	FUNCTION
7~2	-	Reserved
1~0	PWM0.9 ~PWM0.8	The PWM 0 High Bits Register bit 9~8.

PWM 1 High Bits Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	PWM1.9	PWM1.8

Mnemonic: PWM1H Address: D3h

BIT	NAME	FUNCTION
7~2	-	Reserved
1~0	PWM1.9 ~PWM1.8	The PWM1 High Bits Register bit 9~8.

PWM 2 High Bits Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	PWM2.9	PWM2.8

Mnemonic: PWM2H Address: D5h

BIT	NAME	FUNCTION
7~2	-	Reserved
1~0	PWM2.9 ~PWM2.8	The PWM2 High Bits Register bit 9~8.

PWM 3 High Bits Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	PWM3.9	PWM3.8

Mnemonic: PWM3H Address: D6h

BIT	NAME	FUNCTION
7~2	-	Reserved
1~0	PWM3.9 ~PWM3.8	The PWM3 High Bits Register bit 9~8.

PWM Control Register 3

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	BKF

Mnemonic: PWMCON3 Address: D7h

BIT	NAME	FUNCTION
7~1	-	Reserved
0	BKF	The external brake pin Flag. 0: The PWM is not brake. 1: The PWM is brake by external brake pin. It will be cleared by software.

WATCHDOG CONTROL

Bit:	7	6	5	4	3	2	1	0
	WDRUN	-	WD1	WD0	WDIF	WTRF	EWRST	WDCLR

Mnemonic: WDCON Address: D8h

BIT	NAME	FUNCTION
7	WDRUN	0: The Watchdog is stopped. 1: The Watchdog is running.
6	-	Reserved.
5	WD1	Watchdog Timer times selected.
4	WD0	Watchdog Timer times selected.
3	WDIF	Watchdog Timer Interrupt Flag 0: If the interrupt is not enabled, then this bit indicates that the time-out period has elapsed. This bit must be cleared by software. 1: If the watchdog interrupt is enabled, hardware will set this bit to indicate that the watchdog interrupt has occurred.
2	WTRF	Watchdog Timer Reset Flag 1: Hardware will set this bit when the watchdog timer causes a reset. Software can read it but must clear it manually. A power-fail reset will also clear the bit. This bit helps software in determining the cause of a reset. If EWRST = 0, the watchdog timer will have no affect on this bit.
1	EWRST	0: Disable Watchdog Timer Reset. 1: Enable Watchdog Timer Reset.
0	WDCLR	Reset Watchdog Timer This bit helps in putting the watchdog timer into a know state. It also helps in resetting the watchdog timer before a time-out occurs. Failing to set the EWRST before time-out will cause an interrupt, if EWDI (IE1.4) is set, and 512 clocks after that a watchdog timer reset will be generated if EWRST is set. This bit is self-clearing by hardware.

The WDCON SFR is set to a 0x0000x0B on an reset. WTRF (WDCON.2) is set to a 1 on a Watchdog timer reset, but to a 0 on power on/down resets. WDIF (WDCON.3) is not altered by an external reset. EWRST (WDCON.1) is set to 0 on a Power-on reset and unaffected by other resets.

All the bits in this SFR have unrestricted read access. EWRST, WDIF and WDCLR require Timed Access procedure to write. The remaining bits have unrestricted write accesses. Please refer TA register description.

TA	REG	C7H
WDCON	REG	D8H

```
MOV     TA, #AAH
MOV     TA, #55H
SETB    WDCON.0                         ; Reset watchdog timer
ORL     WDCON, #00110000B  ; Select 26 bits watchdog timer
MOV     TA, #AAH
MOV     TA, #55H
ORL     WDCON, #00000010B  ; Enable watchdog
```

PWM Counter Low Bits Register

Bit:	7	6	5	4	3	2	1	0
	PWMP.7	PWMP.6	PWMP.5	PWMP.4	PWMP.3	PWMP.2	PWMP.1	PWMP.0

Mnemonic: PWMPL Address: D9h

BIT	NAME	FUNCTION
7~0	PWMP.7 ~PWMP.0	PWM Counter Low Bits Register.

PWM 0 Low Bits Register

Bit:	7	6	5	4	3	2	1	0
	PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.0

Mnemonic: PWM0L Address: DAh

BIT	NAME	FUNCTION
7~0	PWM0.7 ~PWM0.0	PWM 0 Low Bits Register.

PWM 1 Low Bits Register

Bit:	7	6	5	4	3	2	1	0
	PWM1.7	PWM1.6	PWM1.5	PWM1.4	PWM1.3	PWM1.2	PWM1.1	PWM1.0

Mnemonic: PWM1l Address: DBh

BIT	NAME	FUNCTION
7~0	PWM1.7 ~PWM1.0	PWM 1 Low Bits Register.

PWM Control Register 1

Bit:	7	6	5	4	3	2	1	0
	PWMRUN	Load	CF	CLRPWM	PWM3I	PWM2I	PWM1I	PWM0I

Mnemonic: PWMCON1 Address: DCh

BIT	NAME	FUNCTION
7	PWMRUN	0: The PWM is not running. 1: The PWM counter is running.
6	Load	0: The registers value of PWMP and Comparators are never loaded to counter and Comparator registers. 1: The PWMP register will be load value to counter register after counter underflow, and hardware will clear by next clock cycle.
5	CF	0: The 10-bit counter down count is not underflow. 1: The 10-bit counter down count is underflow. It will be cleared by software.
4	CLRPWM	1: Clear 10-bit PWM counter to 000H.
3	PWM3I	0: PWM3 out is non-inverted. 1: PWM3 output is inverted.
2	PWM2I	0: PWM2 out is non-inverted. 1: PWM2 output is inverted.
1	PWM1I	0: PWM1 out is non-inverted. 1: PWM1 output is inverted.
0	PWM0I	0: PWM0 out is non-inverted. 1: PWM0 output is inverted.

PWM 2 Low Bits Register

Bit:	7	6	5	4	3	2	1	0
	PWM2.7	PWM2.6	PWM2.5	PWM2.4	PWM2.3	PWM2.2	PWM2.1	PWM2.0

Mnemonic: PWM2L Address: DDh

BIT	NAME	FUNCTION
7~0	PWM2.7 ~PWM2.0	PWM 2 Low Bits Register.

PWM 3 Low Bits Register

Bit:	7	6	5	4	3	2	1	0
	PWM3.7	PWM3.6	PWM3.5	PWM3.4	PWM3.3	PWM3.2	PWM3.1	PWM3.0

Mnemonic: PWM3L Address: DEh

BIT	NAME	FUNCTION
7~0	PWM3.7 ~PWM3.0	PWM 3 Low Bits Register.

PWM Control Register 2

Bit:	7	6	5	4	3	2	1	0
	BKCH	BKPS	BPEN	BKEN	PWM3B	PWM2B	PWM1B	PWM0B

Mnemonic: PWMCON2 Address: DFh

BIT	NAME	FUNCTION
7	BKCH	See the below table, when BKEN is set.
6	BKPS	0: Brake is asserted if P0.2 is low. 1: Brake is asserted if P0.2 is high
5	BPEN	See the below table, when BKEN is set.
4	BKEN	0: The Brake is never asserted. 1: The Brake is enabled, and see the below table.
3	PWM3B	0: The PWM3 output is low, when Brake is asserted. 1: The PWM3 output is high, when Brake is asserted.
2	PWM2B	0: The PWM2 output is low, when Brake is asserted. 1: The PWM2 output is high, when Brake is asserted.
1	PWM1B	0: The PWM1 output is low, when Brake is asserted. 1: The PWM1 output is high, when Brake is asserted.
0	PWM0B	0: The PWM0 output is low, when Brake is asserted. 1: The PWM0 output is high, when Brake is asserted.

Brake Condition Table

BPEN	BKCH	BRAKE CONDITION
0	0	Brake On, software brake by BKEN.
0	1	On, when PWM is not running(PWMRUN=0), the PWM output condition is follow PWMnB setting. Off, when PWM is running(PWMRUN=1).
1	0	Brake On, when Brake Pin asserted, no PWM output, the bit of PWMRUN will be cleared and BKF flag will be set.
1	1	No any active.

ACCUMULATOR

Bit:	7	6	5	4	3	2	1	0
	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0

Mnemonic: ACC Address: E0h

ACC.7-0: The A (or ACC) register is the standard 8052 accumulator.

ADC CONTROL REGISTER

Bit:	7	6	5	4	3	2	1	0
	ADC.1	ADC.0	ADCEX	ADCI	ADCS	RCCLK	AADR1	AADR0

Mnemonic: ADCCON Address: E1h

BIT	NAME	FUNCTION
7	ADC.1	The ADC conversion result.
6	ADC.0	The ADC conversion result.
5	ADCEX	Enable STADC-triggered conversion 0: Conversion can only be started by software (i.e., by setting ADCS). 1: Conversion can be started by software or by a rising edge on STADC (pin P1.4).
4	ADCI	ADC Interrupt flag: This flag is set when the result of an A/D conversion is ready. This generates an ADC interrupt, if it is enabled. The flag may be cleared by the ISR. While this flag is 1, the ADC cannot start a new conversion. ADCI can not be set by software.
3	ADCS	ADC Start and Status: Set this bit to start an A/D conversion. It may also be set by STADC if ADCEX is 1. This signal remains high while the ADC is busy and is reset right after ADCI is set. ADCS can not be reset by software, and the ADC cannot start a new conversion while ADCS is high. **ADCI / ADCS / ADC Status** 0 / 0 / ADC not busy; a conversion can be started 0 / 1 / ADC busy; start of a new conversion is blocked 1 / 0 / Conversion completed; start of a new conversion requires ADCI=0 1 / 1 / Conversion completed; start of a new conversion requires ADCI=0 It is recommended to clear ADCI ***before*** ADCS is set. However, if ADCI is cleared and ADCS is set at the same time, a new A/D conversion may start on the same channel.
2	RCCLK	0: The CPU clock is used as ADC clock. 1: The internal RC clock is used as ADC clock.
1	AADR1	The ADC input select. See table below.
0	AADR0	The ADC input select. See table below.

AADR1, AADR0: ADC Analog Input Channel select bits:

These bits can only be changed when ADCI and ADCS are both zero.

AADR1	AADR0	SELECTED ANALOG INPUT CHANNEL
0	0	AD0 (P0.3)
0	1	AD1 (P0.4)
1	0	AD2 (P0.5)
1	1	AD3 (P0.6)

ADC CONVERTER RESULT REGISTER

Bit:	7	6	5	4	3	2	1	0
	ADC.9	ADC.8	ADC.7	ADC.6	ADC.5	ADC.4	ADC.3	ADC.2

Mnemonic: ADCH Address: E2h

BIT	NAME	FUNCTION
7~0	ADC.9 ~ADC.2	The ADC conversion result.

Interrupt Enable Register 1

Bit:	7	6	5	4	3	2	1	0
	-	-	EPWM	EWDI	EC2	EC1	EKB	EI2

Mnemonic: IE1 Address: E8h

BIT	NAME	FUNCTION
7	-	Reserved.
6	-	Reserved.
5	EPWM	0: Disable PWM Interrupt when external brake pin was brake. 1: Enable PWM Interrupt when external brake pin was brake.
4	EWDI	0: Disable Watchdog Timer Interrupt. 1: Enable Watchdog Timer Interrupt.
3	EC2	0: Disable Comparator 2 Interrupt. 1: Enable Comparator 2 Interrupt.
2	EC1	0: Disable Comparator 1 Interrupt. 1: Enable Comparator 1 Interrupt.
1	EKB	0: Disable Keypad Interrupt. 1: Enable Keypad Interrupt.
0	EI2	0: Disable I2C Interrupt. 1: Enable I2C Interrupt.

B REGISTER

Bit:	7	6	5	4	3	2	1	0
	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0

Mnemonic: B Address: F0h

B.7-0: The B register is the standard 8052 register that serves as a second accumulator.

Port 0 Digital Input Disable

Bit:	7	6	5	4	3	2	1	0
	P0ID.7	P0ID.6	P0ID.5	P0ID.4	P0ID.3	P0ID.2	P0ID.1	P0ID.0

Mnemonic: P0ID Address: F6h

BIT	NAME	FUNCTION
7~0	P0ID.7 ~P0ID.0	Enable/Disable Port 0 digital inputs. 0: Enable Port 0 digital inputs. 1: Disable Port 0 digital inputs.

Interrupt High Priority 1

Bit:	7	6	5	4	3	2	1	0
	-	-	PPWMH	PWDIH	PC2H	PC1H	PKBH	PI2H

Mnemonic: IP1H Address: F7h

BIT	NAME	FUNCTION
7	-	Reserved.
6	-	Reserved.
5	PPWMH	1: To set interrupt high priority of PWM's brake is highest priority level.
4	PWDIH	1: To set interrupt high priority of Watchdog is highest priority level.
3	PC2H	1: To set interrupt high priority of Comparator 2 is highest priority level.
2	PC1H	1: To set interrupt high priority of Comparator 1 is highest priority level.
1	PKBH	1: To set interrupt high priority of Keypad is highest priority level.
0	PI2H	1: To set interrupt high priority of I2C is highest priority level.

Interrupt Priority 1

Bit:	7	6	5	4	3	2	1	0
	-	-	PPWM	PWDI	PC2	PC1	PKB	PI2

Mnemonic: IP1 Address: F8h

BIT	NAME	FUNCTION
7	-	Reserved.
6	-	Reserved.
5	PPWM	1: To set interrupt priority of PWM's external brake is higher priority level.
4	PWDI	1: To set interrupt priority of Watchdog is higher priority level.
3	PC2	1: To set interrupt priority of Comparator 2 is higher priority level.
2	PC1	1: To set interrupt priority of Comparator 1 is higher priority level.
1	PKB	1: To set interrupt priority of Keypad is higher priority level.
0	PI2	1: To set interrupt priority of I2C is higher priority level.

9. INSTRUCTION

The W79E82X series execute all the instructions of the standard 8052 family. The operation of these instructions, their effect on the flag bits and the status bits is exactly the same. However, timing of these instructions is different. The reason for this is two fold. Firstly, in the W79E82X series, each machine cycle consists of 4 clock periods, while in the standard 8052 it consists of 12 clock periods. Also, in the W79E82X series there is only one fetch per machine cycle i.e. 4 clocks per fetch, while in the standard 8052 there can be two fetches per machine cycle, which works out to 6 clocks per fetch.

The advantage the W79E82X series has is that since there is only one fetch per machine cycle, the number of machine cycles in most cases is equal to the number of operands that the instruction has. In case of jumps and calls there will be an additional cycle that will be needed to calculate the new address. But overall the W79E82X serial reduces the number of dummy fetches and wasted cycles, thereby improving efficiency as compared to the standard 8052.

TABLE: INSTRUCTIONS AFFECT FLAG SETTING

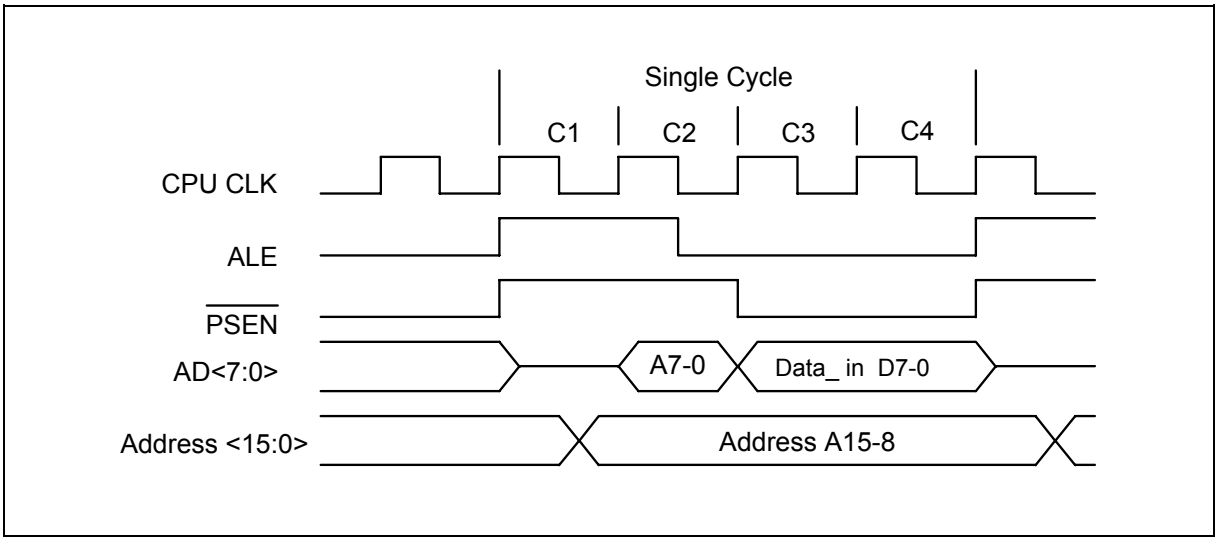
INSTRUCTION	CARRY	OVERFLOW	AUXILIARY CARRY	INSTRUCTION	CARRY	OVERFLOW	AUXILIARY CARRY
ADD	X	X	X	CLR C	0		
ADDC	X	X	X	CPL C	X		
SUBB	X	X	X	ANL C, bit	X		
MUL	0	X		ANL C, bit	X		
DIV	0	X		ORL C, bit	X		
DA A	X			ORL C, bit	X		
RRC A	X			MOV C, bit	X		
RLC A	X			CJNE	X		
SETB C	1						

A "X" indicates that the modification is as per the result of instruction.

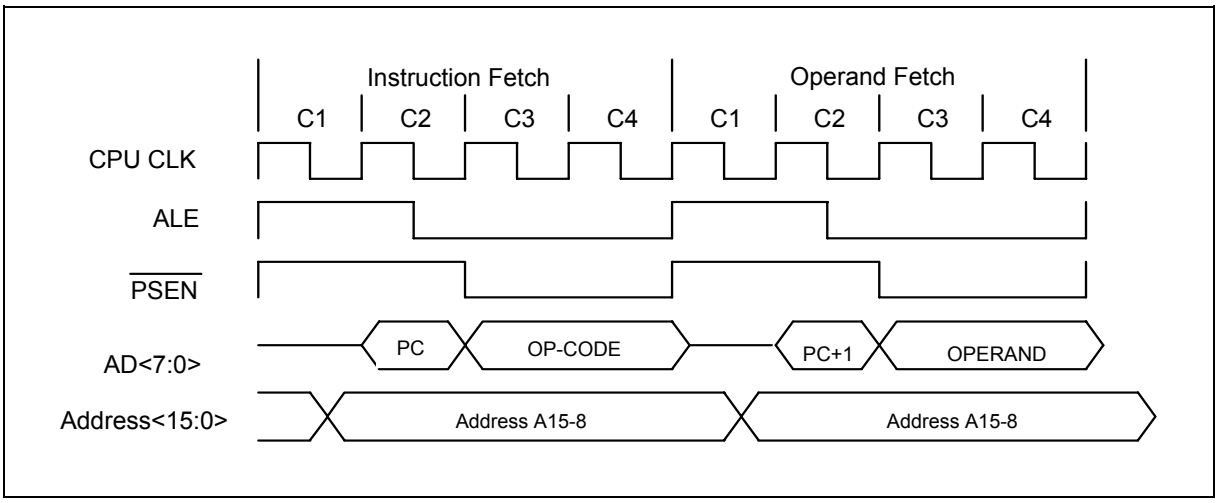
9.1 INSTRUCTION TIMING

The instruction timing for the W79E82X series are an important aspect, especially for those users who wish to use software instructions to generate timing delays. Also, it provides the user with an insight into the timing differences between the W79E82X series and the standard 8052. In the W79E82X series each machine cycle is four clock periods long. Each clock period is designated a state. Thus each machine cycle is made up of four states, C1, C2, C3 and C4, in that order. Due to the reduced time for each instruction execution, both the clock edges are used for internal timing. Hence it is important that the duty cycle of the clock be as close to 50% as possible to avoid timing conflicts. As mentioned earlier, the W79E82X series does one op-code fetch per machine cycle.

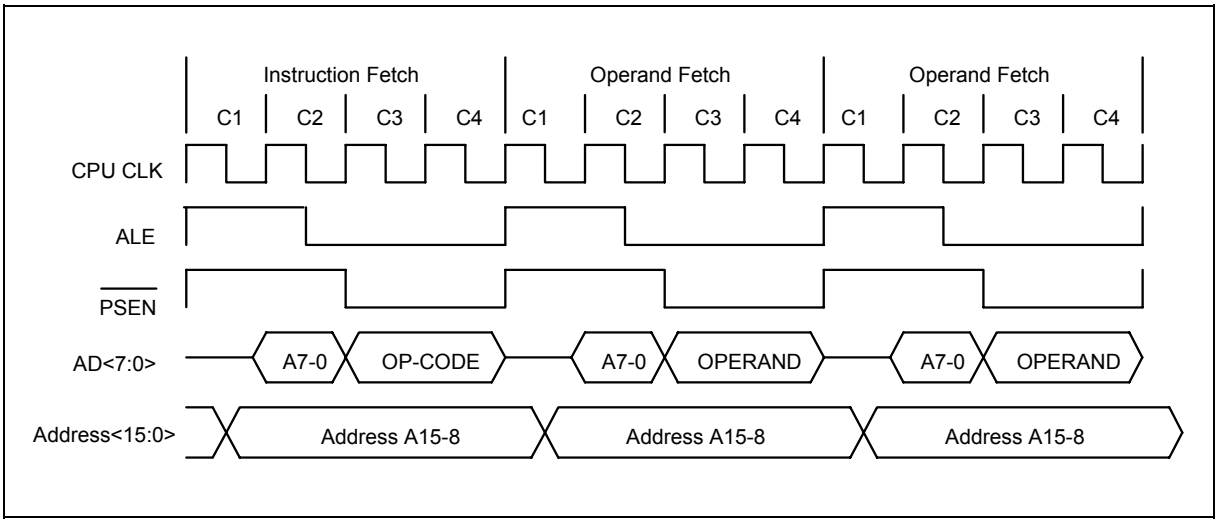
Therefore, in most of the instructions, the number of machine cycles needed to execute the instruction is equal to the number of bytes in the instruction. Of the 256 available op-codes, 128 of them are single cycle instructions. Thus more than half of all op-codes in the W79E82X series are executed in just four clock periods. Most of the two-cycle instructions are those that have two byte instruction codes. However there are some instructions that have only one byte instructions, yet they are two cycle instructions. One instruction which is of importance is the MOVX instruction. In the standard 8052, the MOVX instruction is always two machine cycles long. However, in the W79E82X series each machine cycle is made of only 4 clock periods compared to the 12 clock periods for the standard 8052. Therefore, even though the number of categories has increased, each instruction is at least 1.5 to 3 times faster than the standard 8052 in terms of clock periods.



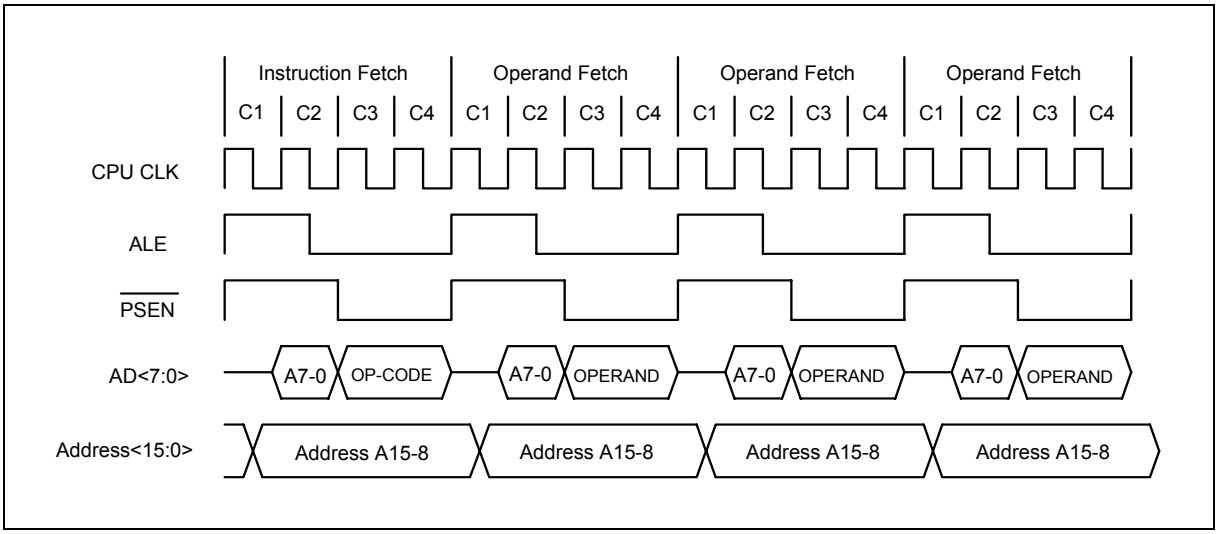
Single Cycle Instruction Timing



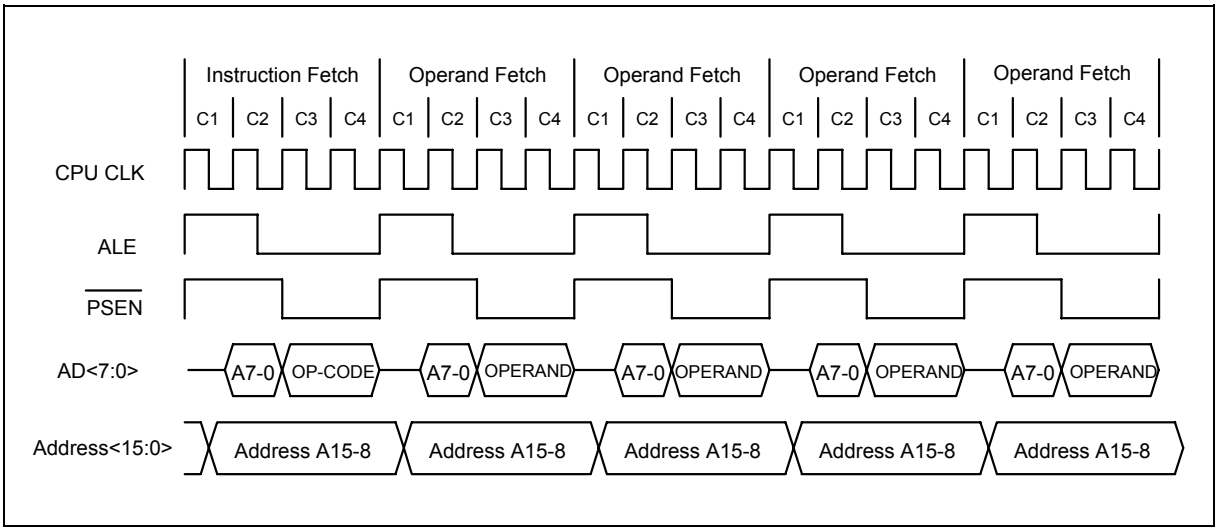
Two Cycle Instruction Timing



Three Cycle Instruction Timing



Four Cycle Instruction Timing



Five Cycle Instruction Timing

10. POWER MANAGEMENT

The W79E82X series provide idle mode and power-down mode to control power consumption. These modes are discussed in the next two sections, followed by a discussion of resets.

10.1 Idle Mode

The user can put the device into idle mode by writing 1 to the bit PCON.0. The instruction that sets the idle bit is the last instruction that will be executed before the device goes into Idle Mode. In the Idle mode, the clock to the CPU is halted, but not to the Interrupt, Timer, Watchdog timer and Serial port blocks. This forces the CPU state to be frozen; the Program counter, the Stack Pointer, the Program Status Word, the Accumulator and the other registers hold their contents. The port pins hold the logical states they had at the time Idle was activated. The Idle mode can be terminated in two ways. Since the interrupt controller is still active, the activation of any enabled interrupt can wake up the processor. This will automatically clear the Idle bit, terminate the Idle mode, and the Interrupt Service Routine (ISR) will be executed. After the ISR, execution of the program will continue from the instruction which put the device into Idle Mode.

The Idle mode can also be exited by activating the reset. The device can put into reset either by applying a low on the external RST pin, a Power on reset condition or a Watchdog timer reset. The external reset pin has to be held high for at least two machine cycles i.e. 8 clock periods to be recognized as a valid reset. In the reset condition the program counter is reset to 0000h and all the SFRs are set to the reset condition. Since the clock is already running there is no delay and execution starts immediately. In the Idle mode, the Watchdog timer continues to run, and if enabled, a time-out will cause a watchdog timer interrupt which will wake up the device. The software must reset the Watchdog timer in order to preempt the reset which will occur after 512 clock periods of the time-out. When the W79E82X series are exiting from an Idle Mode with a reset, the instruction following the one which put the device into Idle Mode is not executed. So there is no danger of unexpected writes.

10.2 Power Down Mode

The device can be put into Power Down mode by writing 1 to bit PCON.1. The instruction that does this will be the last instruction to be executed before the device goes into Power Down mode. In the Power Down mode, all the clocks are stopped and the device comes to a halt. All activity is completely stopped and the power consumption is reduced to the lowest possible value. The port pins output the values held by their respective SFRs.

The W79E82X series will exit the Power Down mode with a reset or by an external interrupt pin enabled as level detected. An external reset can be used to exit the Power down state. The low on RST pin terminates the Power Down mode, and restarts the clock. The program execution will restart from 0000h. In the Power down mode, the clock is stopped, so the Watchdog timer cannot be used to provide the reset to exit Power down mode when its clock source is external OSC or crystal.

The W79E82X series can be woken from the Power Down mode by forcing an external interrupt pin activated, provided the corresponding interrupt is enabled, while the global enable(EA) bit is set and the external input has been set to a level detect mode. If these conditions are met, then the high level on the external pin re-starts the oscillator. Then device executes the interrupt service routine for the corresponding external interrupt. After the interrupt service routine is completed, the program execution returns to the instruction after one which put the device into Power Down mode and continues from there. During Power down mode, if AUXR1.LPBOV = 1 and AUXR1.BOD = 0, the internal RC clock will be enabled and hence save power.

11. RESET CONDITIONS

The user has several hardware related options for placing the W79E82X series into reset condition. In general, most register bits go to their reset value irrespective of the reset condition, but there are a few flags whose state depends on the source of reset. The user can use these flags to determine the cause of reset using software.

11.1 External Reset

The device continuously samples the RST pin at state C4 of every machine cycle. Therefore the RST pin must be held for at least 2 machine cycles to ensure detection of a valid RST low. The reset circuitry then synchronously applies the internal reset signal. Thus the reset is a synchronous operation and requires the clock to be running to cause an external reset.

Once the device is in reset condition, it will remain so as long as RST is 0. Even after RST is deactivated, the device will continue to be in reset state for up to two machine cycles, and then begin program execution from 0000h. There is no flag associated with the external reset condition. However since the other two reset sources have flags, the external reset can be considered as the default reset if those two flags are cleared.

11.2 Power-On Reset (POR)

The software must clear the POR flag after reading it. Otherwise it will not be possible to correctly determine future reset sources. If the power fails, i.e. falls below Vrst, then the device will once again go into reset state. When the power returns to the proper operating levels, the device will again perform a power on reset delay and set the POR flag.

11.3 Watchdog Timer Reset

The Watchdog timer is a free running timer with programmable time-out intervals. The user can clear the watchdog timer at any time, causing it to restart the count. When the time-out interval is reached an interrupt flag is set. If the Watchdog reset is enabled and the watchdog timer is not cleared, then 512 clocks from the flag being set, the watchdog timer will generate a reset. This places the device into the reset condition. The reset condition is maintained by hardware for two machine cycles. Once the reset is removed the device will begin execution from 0000h.

11.4 Reset State

Most of the SFRs and registers on the device will go to the same condition in the reset state. The Program Counter is forced to 0000h and is held there as long as the reset condition is applied. However, the reset state does not affect the on-chip RAM. The data in the RAM will be preserved during the reset. However, the stack pointer is reset to 07h, and therefore the stack contents will be lost. The RAM contents will be lost if the V_{DD} falls below approximately 2V, as this is the minimum voltage level required for the RAM to operate normally. Therefore after a first time power on reset the RAM contents will be indeterminate. During a power fail condition, if the power falls below 2V, the RAM contents are lost.

After a reset most SFRs are cleared. Interrupts and Timers are disabled. The Watchdog timer is disabled if the reset source was a POR. The SFRs have FFh written into them which puts the port pins in a high state.

SFR RESET VALUE

SFR NAME	RESET VALUE	SFR NAME	RESET VALUE
P0	11111111B	I2DAT	xxxxxxxxB
SP	00000111B	I2STATUS	00000xxxB
DPL	00000000B	I2TIMER	00000000B
DPH	00000000B	I2CLK	00000000B
PCON	00xx0000B	I2CON	00000000B
TCON	00000000B	I2ADDR	xxxxxxxxB
TMOD	00000000B	TA	00000000B
TL0	00000000B	PSW	00000000B
TL1	00000000B	PWMP1	xxxxxx00B
TH0	00000000B	PWM0H	xxxxxx00B
TH1	00000000B	PWM1H	xxxxxx00B
CKCON	00000000B	PWM2H	xxxxxx00B
P1	1111xx11B	PWM3H	xxxxxx00B
DIVM	00000000B	WDCON	0x000000B
SCON	00000000B	PWMP0	00000000B
SBUF	xxxxxxxxB	PWM0L	00000000B
P2	xxxxx11B	PWM1L	00000000B
KBI	00000000B	PWMCON1	00000000B
AUXR1	00000000B	PWM2L	00000000B
IE	00000000B	PWM3L	00000000B
SADDR	00000000B	PWMCON2	00000000B
CMP1	00000000B	ACC	00000000B
CMP2	00000000B	ADCCON	xx000x00B
P0M1	00000000B	ADCH	xxxxxxxxB
P0M2	00000000B	IE1	xx000000B
P1M1	00000000B	B	00000000B
P1M2	00000000B	P0IDS	00000000B
P2M1	00000000B	IPH	xx000000B
P2M2	xxxxxx00B	IP1	xx000000B
IP0H	x0000000B		
IP0	x0000000B		
SADEN	00000000B		

The WDCON SFR bits are set/cleared in reset condition depending on the source of the reset.

	External reset	Watchdog reset	Power on reset
WDCON	0x0x0xx0B	0x0x01x0B	01000000B

The WTRF bit WDCON.2 is set when the Watchdog timer causes a reset. A power on reset will also clear this bit. The EWRST bit WDCON.1 is cleared by power on resets. This disables the Watchdog timer resets. A watchdog or external reset does not affect the EWRST bit.

12. INTERRUPTS

The W79E82X series have four priority level interrupts structure with 13 interrupt sources. Each of the interrupt sources has an individual priority bit, flag, interrupt vector and enable bit. In addition, the interrupts can be globally enabled or disabled.

12.1 Interrupt Sources

The External Interrupts $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ can be either edge triggered or level triggered, depending on bits IT0 and IT1. The bits IE0 and IE1 in the TCON register are the flags which are checked to generate the interrupt. In the edge triggered mode, the INTx inputs are sampled in every machine cycle. If the sample is high in one cycle and low in the next, then a high to low transition is detected and the interrupts request flag IEx in TCON is set. The flag bit requests the interrupt. Since the external interrupts are sampled every machine cycle, they have to be held high or low for at least one complete machine cycle. The IEx flag is automatically cleared when the service routine is called. If the level triggered mode is selected, then the requesting source has to hold the pin low till the interrupt is serviced. The IEx flag will not be cleared by the hardware on entering the service routine. If the interrupt continues to be held low even after the service routine is completed, then the processor may acknowledge another interrupt request from the same source.

The Timer 0 and 1 Interrupts are generated by the TF0 and TF1 flags. These flags are set by the overflow in the Timer 0 and Timer 1. The TF0 and TF1 flags are automatically cleared by the hardware when the timer interrupt is serviced. The Watchdog timer can be used as a system monitor or a simple timer. In either case, when the time-out count is reached, the Watchdog Timer interrupt flag WDIF (WDCON.3) is set. If the interrupt is enabled by the enable bit IE1.4, then an interrupt will occur.

The Serial block can generate interrupt on reception or transmission. There are two interrupt sources from the Serial block, which are obtained by the RI and TI bits in the SCON SFR. These bits are not automatically cleared by the hardware, and the user will have to clear these bits using software.

All the bits that generate interrupts can be set or reset by hardware, and thereby software initiated interrupts can be generated. Each of the individual interrupts can be enabled or disabled by setting or clearing a bit in the IE SFR. IE also has a global enable/disable bit EA, which can be cleared to disable all interrupts.

The ADC can generate interrupt after finished ADC converter. There is one interrupt source, which is obtained by the ADCI bit in the ADCCON SFR. This bit is not automatically cleared by the hardware, and the user will have to clear this bit using software.

The two comparators can generate interrupt after comparator output has toggle occurs by CMF1 and CMF2. These bits are not automatically cleared by the hardware, and the user will have to clear these bits using software.

The I2C function can generate interrupt by SI flag, after I2C finished some action, then SI will set by hardware. If interrupt of I2C is enabled, it will generate interrupt. This bit will clear by software.

The PWM function can generate interrupt by BKF flag, after external brake pin has brake occurred. This bit will clear by software.

12.2 Priority Level Structure

There are four priority levels for the interrupts, highest, high, low and lowest. The interrupt sources can be individually set to either high or low levels. Naturally, a higher priority interrupt cannot be interrupted by a lower priority interrupt. However there exists a pre-defined hierarchy amongst the interrupts themselves. This hierarchy comes into play when the interrupt controller has to resolve simultaneous requests having the same priority level. This hierarchy is defined as shown below; the interrupts are numbered starting from the highest priority to the lowest.

Priority structure of interrupts

SOURCE	FLAG	PRIORITY LEVEL
External Interrupt 0	IE0	1(highest)
Brownout Detect	BOF	2
Watchdog Timer	WDIF	3
Timer 0 Overflow	TF0	4
I2C Interrupt	SI	5
ADC Interrupt	ADCI	6
External Interrupt 1	IE1	7
KBI Interrupt	KBF	8
Comparator 1 Interrupt	CMF1	9
Timer 1 Overflow	TF1	10
Comparator 2 Interrupt	CMF2	11
Serial Port	RI + TI	12
PWM	BKF	13 (lowest)

The interrupt flags are sampled every machine cycle. In the same machine cycle, the sampled interrupts are polled and their priority is resolved. If certain conditions are met then the hardware will execute an internally generated LCALL instruction which will vector the process to the appropriate interrupt vector address. The conditions for generating the LCALL are

1. An interrupt of equal or higher priority is not currently being serviced.

2. The current polling cycle is the last machine cycle of the instruction currently being execute.

3. The current instruction does not involve a write to IE, IE1, IP0, IP0H, IP1 or IPH1 registers and is not a RETI.

If any of these conditions are not met, then the LCALL will not be generated. The polling cycle is repeated every machine cycle, with the interrupts sampled in the same machine cycle. If an interrupt flag is active in one cycle but not responded to, and is not active when the above conditions are met, the denied interrupt will not be serviced. This means that active interrupts are not remembered; every polling cycle is new.

The processor responds to a valid interrupt by executing an LCALL instruction to the appropriate service routine. This may or may not clear the flag which caused the interrupt. In case of Timer interrupts, the TF0 or TF1 flags are cleared by hardware whenever the processor vectors to the appropriate timer service routine. In case of external interrupt, INT0 and INT1, the flags are cleared only if they are edge triggered. In case of Serial interrupts, the flags are not cleared by hardware. The Watchdog timer interrupt flag WDIF has to be cleared by software. The hardware LCALL behaves exactly like the software LCALL instruction. This instruction saves the Program Counter contents onto the Stack, but does not save the Program Status Word PSW. The PC is reloaded with the vector address of that interrupt which caused the LCALL. These address of vector for the different sources are as follows

Vector locations for interrupt sources

SOURCE	VECTOR ADDRESS	SOURCE	VECTOR ADDRESS
External Interrupt 0	0003h	Timer 0 Overflow	000Bh
External Interrupt 1	0013h	Timer 1 Overflow	001Bh
Serial Port	0023h	Brownout Interrupt	002Bh
I2C Interrupt	0033h	KBI Interrupt	003Bh
Comparator 2 Interrupt	0043h	-	004Bh
Watchdog Timer	0053h	ADC Interrupt	005Bh
Comparator 1 Interrupt	0063h	-	006Bh
PWM Brake Interrupt	0073h	-	007Bh

Four-level interrupt priority

PRIORITY BITS		INTERRUPT PRIORITY LEVEL
IPXH	IPX	
0	0	Level 0 (lowest priority)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (highest priority)

The vector table is not evenly spaced; this is to accommodate future expansions to the device family.

Execution continues from the vectored address till an RETI instruction is executed. On execution of the RETI instruction the processor pops the Stack and loads the PC with the contents at the top of the stack. The user must take care that the status of the stack is restored to what is was after the hardware LCALL, if the execution is to return to the interrupted program. The processor does not notice anything if the stack contents are modified and will proceed with execution from the address put back into PC. Note that a RET instruction would perform exactly the same process as a RETI instruction, but it would not inform the Interrupt Controller that the interrupt service routine is completed, and would leave the controller still thinking that the service routine is underway.

The W79E82X series use a four priority level interrupt structure. This allows great flexibility in controlling the handling of the W79E82X series many interrupt sources. The W79E82X series supports up to 13 interrupt sources.

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in registers IE0 or IE1. The IE0 register also contains a global disable bit, EA, which disables all interrupts at once.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the IP0, IP0H, IP1, and IP1H registers. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. So, if two requests of different priority levels are received simultaneously, the request of higher priority level is serviced.

If requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve simultaneous requests of the same priority level.

As below Table summarizes the interrupt sources, flag bits, vector addresses, enable bits, priority bits, arbitration ranking, and whether each interrupt may wake up the CPU from Power Down mode.

DESCRIPTION	INTERRUPT FLAG BIT(S)	VECTOR ADDRESS	INTERRUPT ENABLE BIT(S)	INTERRUPT PRIORITY	ARBITRATION RANKING	POWER DOWN WAKEUP
External Interrupt 0	IE0	0003H	EX0 (IE0.0)	IP0H.0, IP0.0	1(highest)	Yes
Brownout Detect	BOF	002BH	EBO (IE.5)	IP0H.5, IP0.5	2	Yes
Watchdog Timer	WDIF	0053H	EWDI (IE1.4)	IP1H.4, IP1.4	3	Yes(1)
Timer 0 Interrupt	TF0	000BH	ET0 (IE.1)	IP0H.1, IP0.1	4	No
I2C Interrupt	SI	0033H	EI2 (IE1.0)	IP1H.0, IP1.0	5	No
ADC Converter	ADCI	005BH	EAD (IE.6)	IP0H.6, IP0.6	6	Yes(1)
External Interrupt 1	IE1	0013H	EX1 (IE.2)	IP0H.2, IP0.2	7	Yes
KBI Interrupt	KBF	003BH	EKB (IE1.1)	IP1H.1, IP1.1	8	Yes
Comparator 1 Interrupt	CMF1	0063H	EC1 (IE1.2)	IP1H.2, IP1.2	9	Yes
Timer 1 Interrupt	TF1	001BH	ET1 (IE.3)	IP0H.3, IP0.3	10	No
Comparator 2 Interrupt	CMF2	0043H	EC2 (IE1.3)	IP1H.3, IP1.3	11	Yes
Serial Port Tx and Rx	TI & RI	0023H	ES (IE.4)	IP0H.4, IP0.4	12	No
PWM Interrupt	BKF	0073H	EPWM (IE1.5)	IP1H.5, IP1.5	13 (lowest)	No

Note: 1. The Watchdog Timer and ADC Converter can wake up Power Down Mode when its clock source is used internal RC.

12.3 Interrupt Response Time

The response time for each interrupt source depends on several factors, such as the nature of the interrupt and the instruction underway. In the case of external interrupts $\overline{\text{INT0}}$ to RI+TI, they are sampled at C3 of every machine cycle and then their corresponding interrupt flags IEx will be set or reset. The Timer 0 and 1 overflow flags are set at C3 of the machine cycle in which overflow has occurred. These flag values are polled only in the next machine cycle. If a request is active and all three conditions are met, then the hardware generated LCALL is executed. This LCALL itself takes four machine cycles to be completed. Thus there is a minimum time of five machine cycles between the interrupt flag being set and the interrupt service routine being executed.

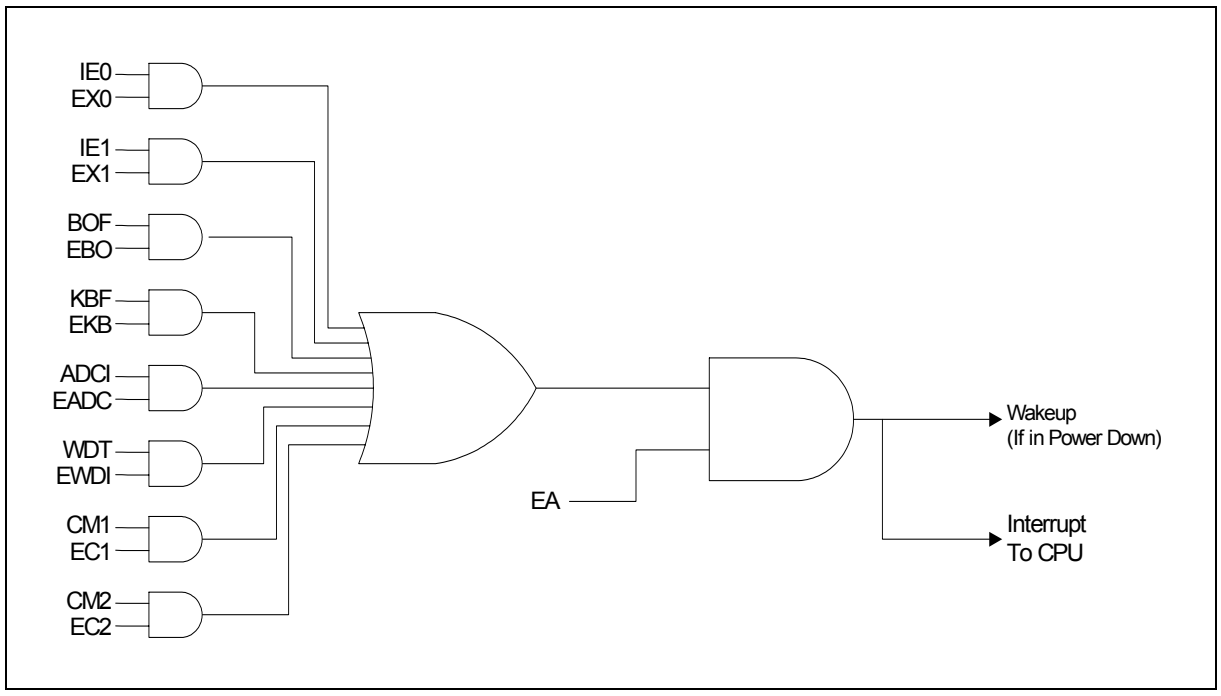
A longer response time should be anticipated if any of the three conditions are not met. If a higher or equal priority is being serviced, then the interrupt latency time obviously depends on the nature of the service routine currently being executed. If the polling cycle is not the last machine cycle of the instruction being executed, then an additional delay is introduced. The maximum response time (if no other interrupt is in service) occurs if the W79E82X series are performing a write to IE, IE1, IP0, IP0H, IP1 or IP1H and then executes a MUL or DIV instruction. From the time an interrupt source is activated, the longest reaction time is 12 machine cycles. This includes 1 machine cycle to detect the interrupt, 2 machine cycles to complete the IE, IE1, IP0, IP0H, IP1 or IP1H access, 5 machine cycles to complete the MUL or DIV instruction and 4 machine cycles to complete the hardware LCALL to the interrupt vector location.

Thus in a single-interrupt system the interrupt response time will always be more than 5 machine cycles and not more than 12 machine cycles. The maximum latency of 12 machine cycles is 48 clock cycles. Note that in the standard 8051 the maximum latency is 8 machine cycles which equals 96 machine cycles. This is a 50% reduction in terms of clock periods.

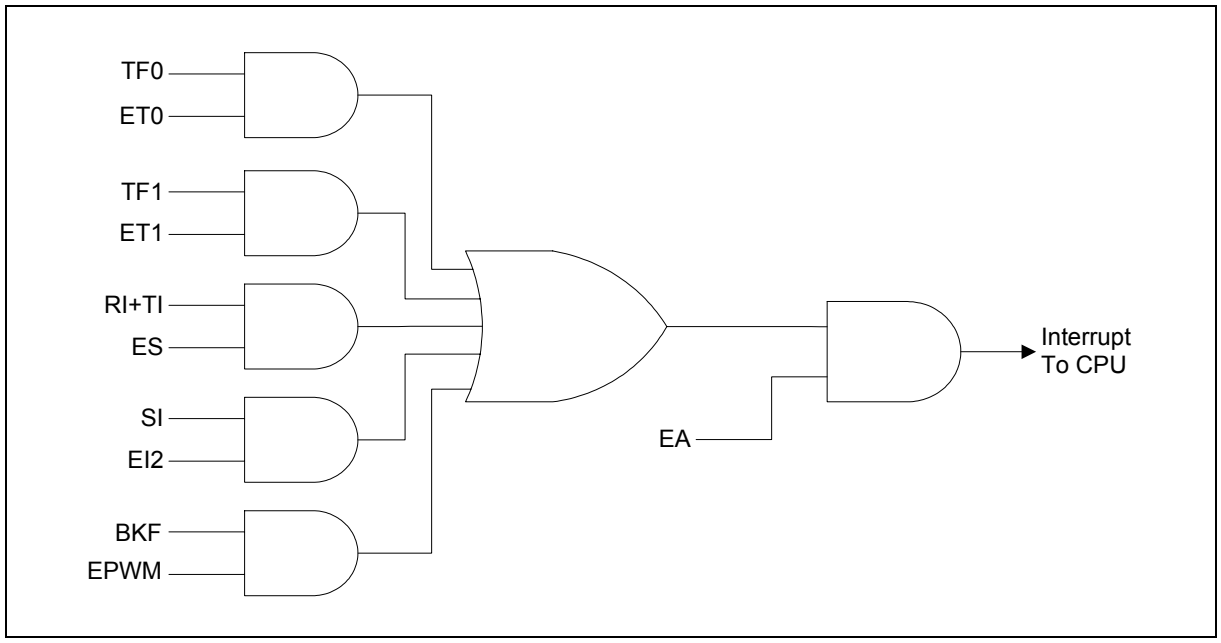
12.4 Interrupt Inputs

The W79E82X series have 13 interrupts source, and two individual interrupt inputs sources, one is for IE0,IE1, BOF, KBF, WDT, ADC, CMF1 and CMF2, and other is IF0, IF1, RI+TI ,SI and BKF. Two interrupt inputs are identical to those present on the standard 80C51 microcontroller as show in below figures.

If an external interrupt is enabled when the W79E82X series are put into Power Down or Idle mode, the interrupt will cause the processor to wake up and resume operation.



As below figure, those interrupt can't be wakeup after Power down.



13. PROGRAMMABLE TIMERS/COUNTERS

The W79E82X series have two 16-bit programmable timer/counters and one programmable Watchdog Timer. The Watchdog Timer is operationally quite different from the other two timers.

13.1 TIMER/COUNTERS 0 & 1

The W79E82X series have two 16-bit Timer/Counters. Each of these Timer/Counters has two 8 bit registers which form the 16 bit counting register. For Timer/Counter 0 they are TH0, the upper 8 bits register, and TL0, the lower 8 bit register. Similarly Timer/Counter 1 has two 8 bit registers, TH1 and TL1. The two can be configured to operate either as timers, counting machine cycles or as counters counting external inputs.

When configured as a "Timer", the timer counts clock cycles. The timer clock can be programmed to be thought of as 1/12 of the system clock or 1/4 of the system clock. In the "Counter" mode, the register is incremented on the falling edge of the external input pin, T0 in case of Timer 0, and T1 for Timer 1. The T0 and T1 inputs are sampled in every machine cycle at C4. If the sampled value is high in one machine cycle and low in the next, then a valid high to low transition on the pin is recognized and the count register is incremented. Since it takes two machine cycles to recognize a negative transition on the pin, the maximum rate at which counting will take place is 1/8 of the master clock frequency. In either the "Timer" or "Counter" mode, the count register will be updated at C3. Therefore, in the "Timer" mode, the recognized negative transition on pin T0 and T1 can cause the count register value to be updated only in the machine cycle following the one in which the negative edge was detected.

The "Timer" or "Counter" function is selected by the "$C/\overline{T}$" bit in the TMOD Special Function Register. Each Timer/Counter has one selection bit for its own; bit 2 of TMOD selects the function for Timer/Counter 0 and bit 6 of TMOD selects the function for Timer/Counter 1. In addition each Timer/Counter can be set to operate in any one of four possible modes. The mode selection is done by bits M0 and M1 in the TMOD SFR.

13.2 Time-Base Selection

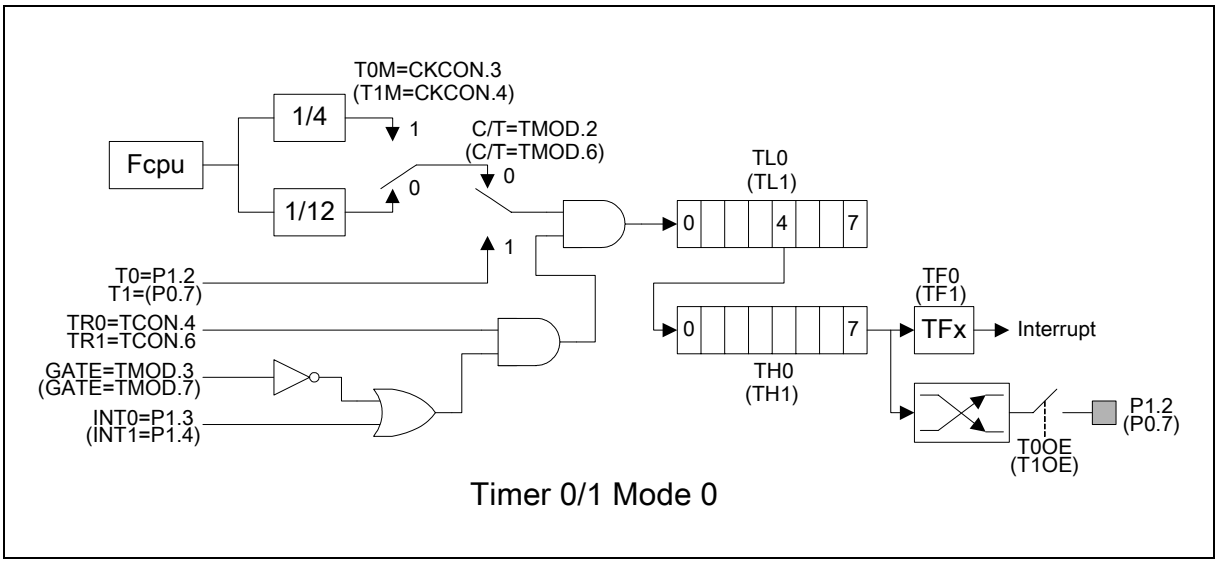
The W79E82X series give the user two modes of operation for the timer. The timers can be programmed to operate like the standard 8051 family, counting at the rate of 1/12 of the clock speed. This will ensure that timing loops on the W79E82X series and the standard 8051 can be matched. This is the default mode of operation of the W79E82X series timers. The user also has the option to count in the turbo mode, where the timers will increment at the rate of 1/4 clock speed. This will straight-away increase the counting speed three times. This selection is done by the T0M and T1M bit in CKCON SFR. A reset sets these bits to 0, and the timers then operate in the standard 8051 mode. The user should set these bits to 1 if the timers are to operate in turbo mode.

13.3 MODE 0

In Mode 0, the timer/counters act as a 8-bit counter with a 5-bit, divide by 32 pre-scale. In this mode we have a 13-bit timer/counter. The 13-bit counter consists of 8 bits of THx and 5 lower bits of TLx. The upper 3 bits of TLx are ignored.

The negative edge of the clock is increments count in the TLx register. When the fifth bit in TLx moves from 1 to 0, then the count in the THx register is incremented. When count in THx moves from FFh to 00h, then the overflow flag TFx in TCON SFR is set. The counted input is enabled only if TRx is set

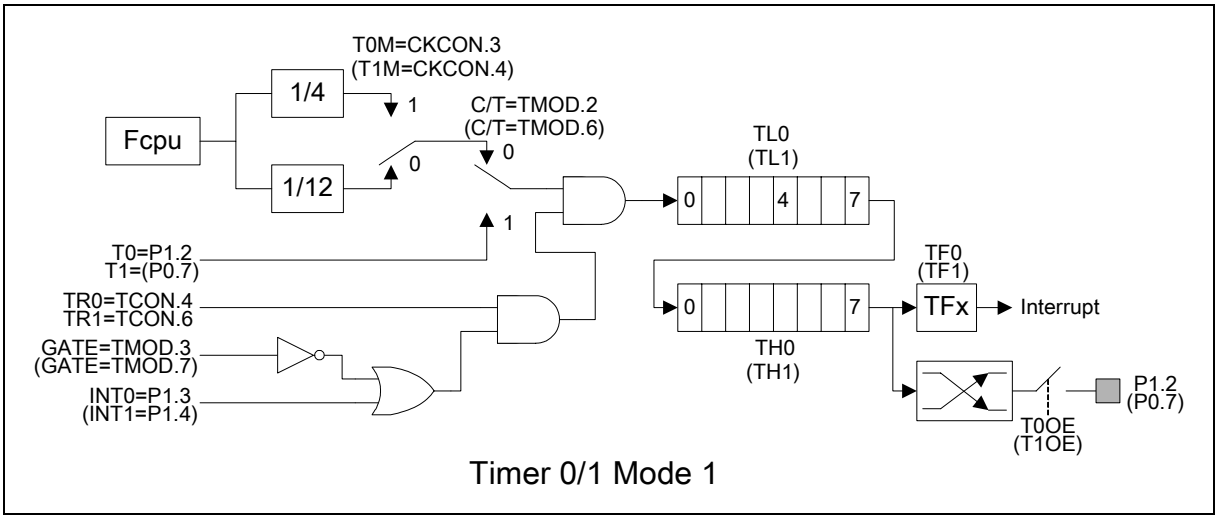
and either GATE = 0 or $\overline{INTx}$ = 1. When C/$\overline{T}$ is set to 0, then it will count clock cycles, and if C/$\overline{T}$ is set to 1, then it will count 1 to 0 transitions on T0 (P1.2) for timer 0 and T1 (P0.7) for timer 1. When the 13-bit count reaches 1FFFh the next count will cause it to roll-over to 0000h. The timer overflow flag TFx of the relevant timer is set and if enabled an interrupts will occur.



Timer /Counter Mode 0

13.4 MODE 1

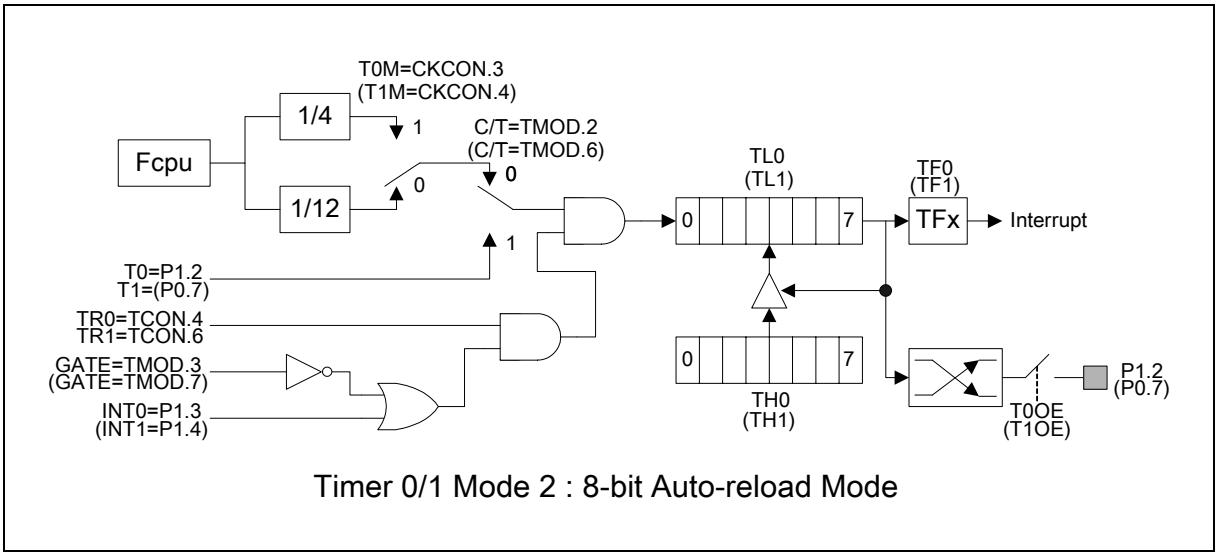
Mode 1 is similar to Mode 0 except that the counting register forms a 16-bit counter, rather than a 13-bit counter. This means that all the bits of THx and TLx are used. Roll-over occurs when the timer moves from a count of FFFFh to 0000h. The timer overflow flag TFx of the relevant timer is set and if enabled an interrupt will occur. The selection of the time-base in the timer mode is similar to that in Mode 0. The gate function operates similarly to that in Mode 0.



Timer/Counter Mode 1

13.5 MODE 2

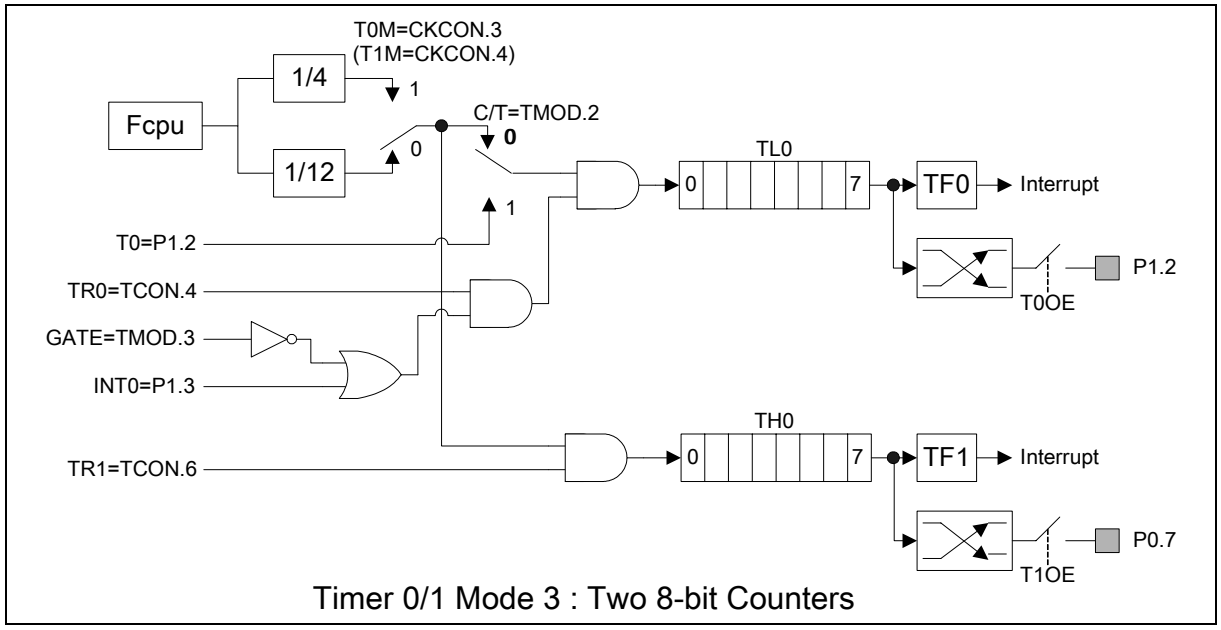
In Mode 2, the timer/counter is in the Auto Reload Mode. In this mode, TLx acts as a 8-bit count register, while THx holds the reload value. When the TLx register overflows from FFh to 00h, the TFx bit in TCON is set and TLx is reloaded with the contents of THx, and the counting process continues from here. The reload operation leaves the contents of the THx register unchanged. Counting is enabled by the TRx bit and proper setting of GATE and $\overline{INTx}$ pins. As in the other two modes 0 and 1 mode 2 allows counting of either clock cycles (clock/12 or clock/4) or pulses on pin Tn.



Timer/Counter Mode 2.

13.6 MODE 3

Mode 3 has different operating methods for the two timer/counters. For timer/counter 1, mode 3 simply freezes the counter. Timer/Counter 0, however, configures TL0 and TH0 as two separate 8 bit count registers in this mode. The logic for this mode is shown in the figure. TL0 uses the Timer/Counter 0 control bits $C/\overline{T}$, GATE, TR0, $\overline{INT0}$ and TF0. The TL0 can be used to count clock cycles (clock/12 or clock/4) or 1-to-0 transitions on pin T0 as determined by C/T (TMOD.2). TH0 is forced as a clock cycle counter (clock/12 or clock/4) and takes over the use of TR1 and TF1 from Timer/Counter 1. Mode 3 is used in cases where an extra 8 bit timer is needed. With Timer 0 in Mode 3, Timer 1 can still be used in Modes 0, 1 and 2., but its flexibility is somewhat limited. While its basic functionality is maintained, it no longer has control over its overflow flag TF1 and the enable bit TR1. Timer 1 can still be used as a timer/counter and retains the use of GATE and INT1 pin. In this condition it can be turned on and off by switching it out of and into its own Mode 3. It can also be used as a baud rate generator for the serial port.



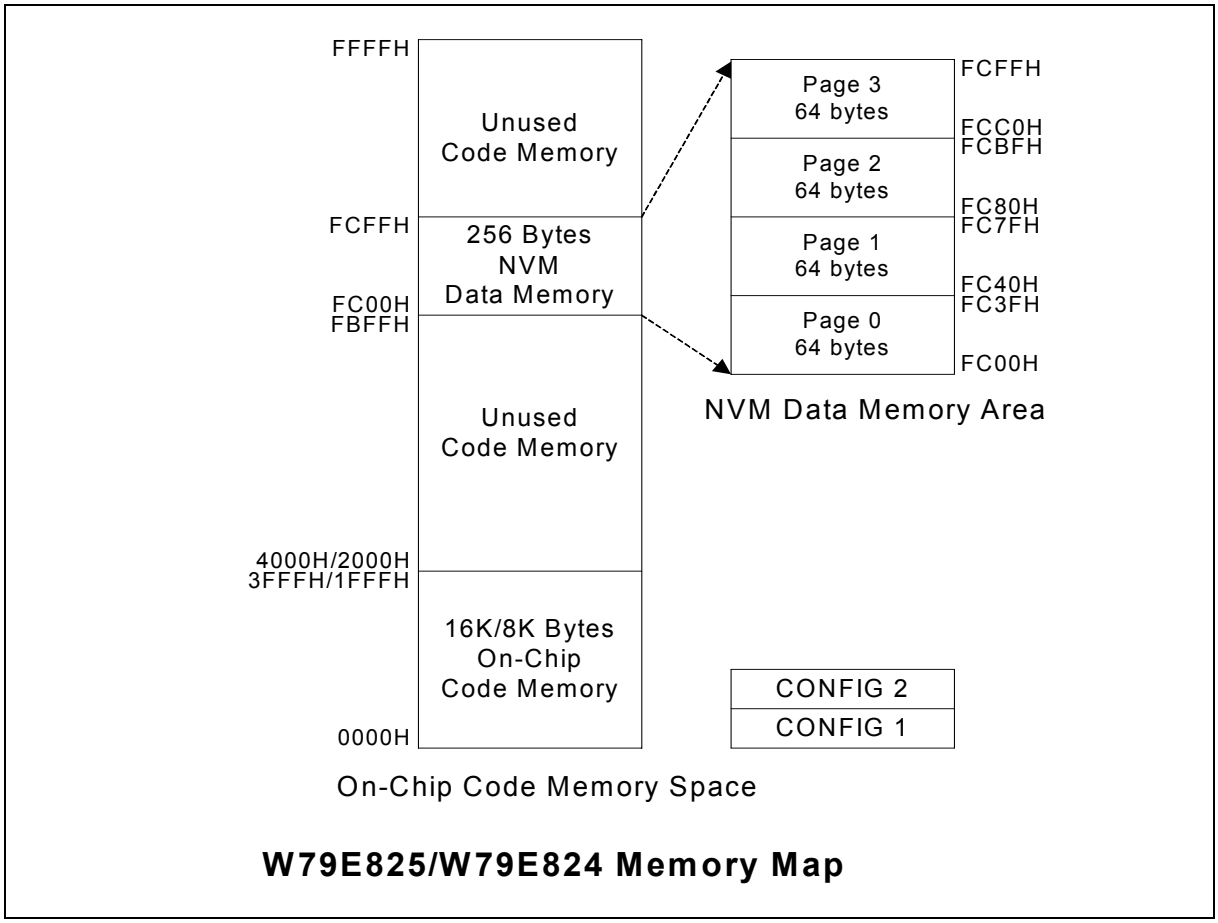
Timer/Counter Mode 3.

14. NVM MEMORY

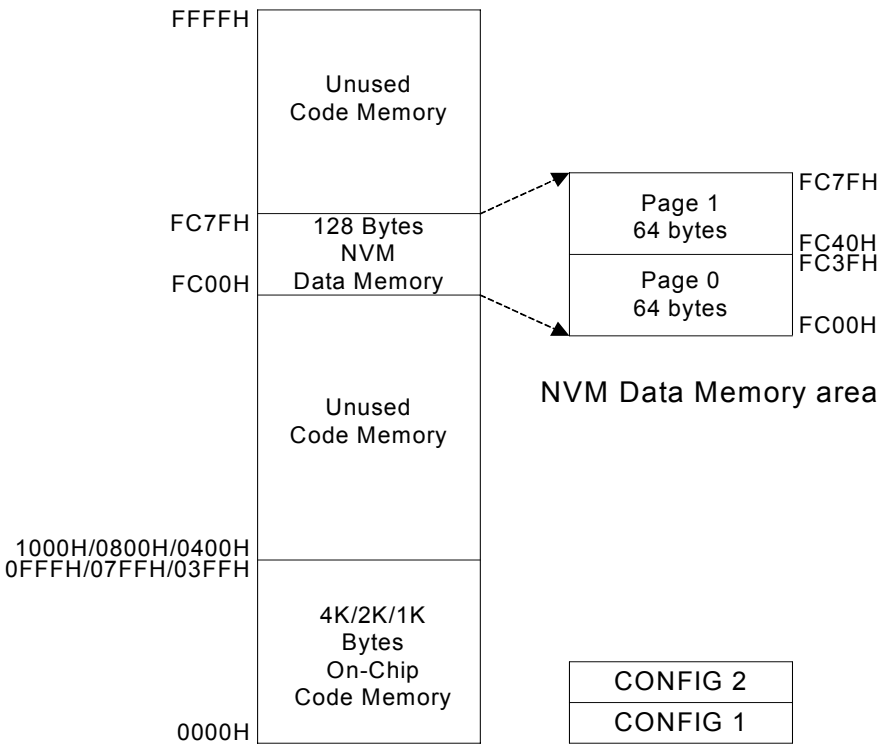
The W79E82X series have NVM data memory of **256/128** bytes for customer's data store used. The NVM data memory has **four/two** pages area and each page has 64 bytes as below figure. The **Page 0** address is from **FC00h ~ FC3Fh**, **Page 1** address is from **FC40h ~ FC7Fh**, **Page 2** address is from **FC80h ~ FCBFh**, and **Page 3** address is from **FCC0h ~ FCFFh**.

The NVM memory can be read/write by customer program to access. Read NVM data is by MOVC A,@A+DPTR instruction, and write data is by SFR of NVMADDR, NVMDAT and NVMCON. Before write data to NVM memory, the page must be erased by set page address which low byte address of On-Chip Code Memory space will decode and enable page(n) on NVMADDR, then set EER of NVMCON.7 will automatically hold fetch program code and PC Counter, and execute page erase. After finished, this bit will be cleared by hardware. The erase time is ~ 5ms.

By write data to NVM memory, user must set address and data to NVMADDR and NVMDAT, therefore set EWR of NVMCON.6 to write data, then uC will hold program code and PC Counter, then write data to mapping address, after finished, this bit will be cleared by hardware, the uC will continue execute next instruction. The program time is ~50us.



W79E825/W79E824 Memory Map



W79E823/W79E822/W79E821 Memory Map

BIT	NAME	FUNCTION
7~0	NVMADDR.7 ~ NVMADDR.0	The NVM address: The register is indicated NVM data memory of low byte address on On-Chip code memory space.

Mnemonic: NVMADDR Address: C6h

BIT	NAME	FUNCTION
7	EER	NVM page(n) erase bit. 0: Without erase NVM Page(n). 1: Set this bit to erase NVM data of page(n) to FFH. The NVM has 4 pages and each page have 64 bytes data memory. Before select page by NVMADDR register that will automatic enable page area, after set this bit, the page will be erased and program counter will halt at this instruction. After finished, program counter will kept next instruction then executed. The NVM page's address define as below table.
6	EWR	NVM data write bit 0: Without write NVM data. 1: Set this bit to write NVM bytes and program counter will halt at this instruction. After write is finished, program counter will kept next instruction then executed.
5~0	-	Reserved

Mnemonic: NVMCON Address: CEh

NVM Page(n) Area Definition Table:

PAGE	START ADDRESS	END ADDRESS
0	00H	3FH
1	40H	7FH
2	***80H***	***BFH***
3	***C0H***	***FFH***

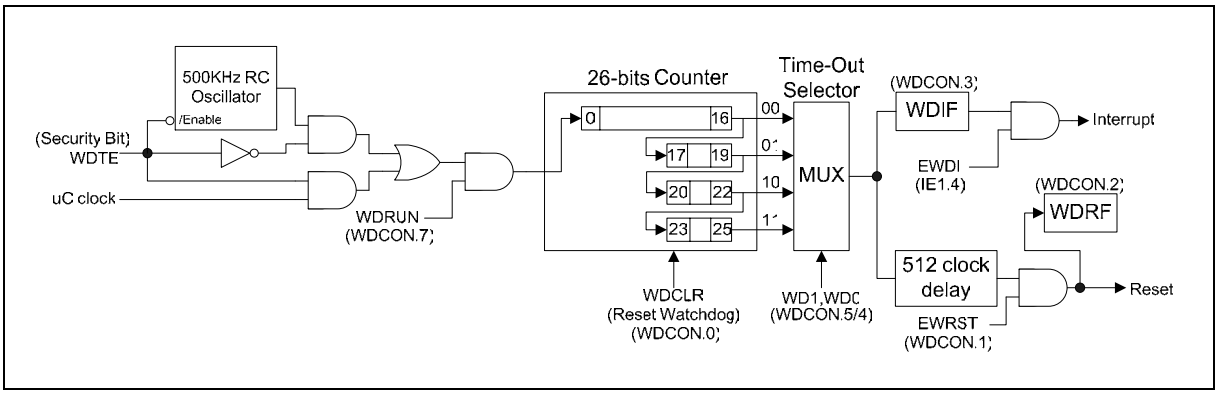
Note: The W79E823, W79E822 and W79E821 without page 2 and page 3.

BIT	NAME	FUNCTION
7~0	NVMDAT.7 ~ NVMDAT.0	The NVM data write register. The read NVM data is by MOVC instruction.

Mnemonic: NVMDATA Address: CFh

15. WATCHDOG TIMER

The Watchdog Timer is a free-running Timer which can be programmed by the user to serve as a system monitor, a time-base generator or an event timer. It is basically a set of dividers that divide the system clock. The divider output is selectable and determines the time-out interval. When the time-out occurs a flag is set, which can cause an interrupt if enabled, and a system reset can also be caused if it is enabled. The interrupt will occur if the individual interrupt enable and the global enable are set. The interrupt and reset functions are independent of each other and may be used separately or together depending on the users software.



Watchdog Timer

The Watchdog Timer should first be restarted by using WDCLR. This ensures that the timer starts from a known state. The WDCLR bit is used to restart the Watchdog Timer. This bit is self clearing, i.e. after writing a 1 to this bit the software will automatically clear it. The Watchdog Timer will now count clock cycles. The time-out interval is selected by the two bits WD1 and WD0 (WDCON.5 and WDCON.4). When the selected time-out occurs, the Watchdog interrupt flag WDIF (WDCON.3) is set. After the time-out has occurred, the Watchdog Timer waits for an additional 512 clock cycles. If the Watchdog Reset EWRST (WDCON.1) is enabled, then 512 clocks after the time-out, if there is no WDCLR, a system reset due to Watchdog Timer will occur. This will last for two machine cycles, and the Watchdog Timer reset flag WDRF (WDCON.2) will be set. This indicates to the software that the Watchdog was the cause of the reset.

When used as a simple timer, the reset and interrupt functions are disabled. The timer will set the WDIF flag each time the timer completes the selected time interval. The WDIF flag is polled to detect a time-out and the WDCLR allows software to restart the timer. The Watchdog Timer can also be used as a very long timer. The interrupt feature is enabled in this case. Every time the time-out occurs an interrupt will occur if the global interrupt enable EA is set.

The main use of the Watchdog Timer is as a system monitor. This is important in real-time control applications. In case of some power glitches or electro-magnetic interference, the processor may begin to execute errant code. If this is left unchecked the entire system may crash. Using the watchdog timer interrupt during software development will allow the user to select ideal watchdog reset locations. The code is first written without the watchdog interrupt or reset. Then the Watchdog interrupt is enabled to identify code locations where interrupt occurs. The user can now insert instructions to reset the Watchdog Timer, which will allow the code to run without any Watchdog Timer

interrupts. Now the Watchdog Timer reset is enabled and the Watchdog interrupt may be disabled. If any errant code is executed now, then the reset Watchdog Timer instructions will not be executed at the required instants and Watchdog reset will occur.

The Watchdog Timer time-out selection will result in different time-out values depending on the clock speed. The reset, when enabled, will occurs 512 clocks after the time-out has occurred.

Time-out values for the Watchdog timer

WD1	WD0	WATCHDOG INTERVAL	NUMBER OF CLOCKS	TIME @ 10 MHZ
0	0	2^{17}	131072	13.11 mS
0	1	2^{20}	1048576	104.86 mS
1	0	2^{23}	8388608	838.86 mS
1	1	2^{26}	67108864	6710.89 mS

The Watchdog Timer will de disabled by a power-on/fail reset. The Watchdog Timer reset does not disable the Watchdog Timer, but will restart it. In general, software should restart the timer to put it into a known state.

The control bits that support the Watchdog Timer are discussed below.

15.1 WATCHDOG CONTROL

WDIF: WDCON.3 - Watchdog Timer Interrupt flag. This bit is set whenever the time-out occurs in the Watchdog Timer. If the Watchdog interrupt is enabled (IE1.4), then an interrupt will occur (if the global interrupt enable is set and other interrupt requirements are met). Software or any reset can clear this bit.

WDRF: WDCON.2 - Watchdog Timer Reset flag. This bit is set whenever a watchdog reset occurs. This bit is useful for determined the cause of a reset. Software must read it, and clear it manually. A Power-fail reset will clear this bit. If EWDRST = 0, then this bit will not be affected by the Watchdog Timer.

EWRST: WDCON.1 - Enable Watchdog Timer Reset. This bit when set to 1 will enable the Watchdog Timer reset function. Setting this bit to 0 will disable the Watchdog Timer reset function, but will leave the timer running.

WDCLR: WDCON.0 - Reset Watchdog Timer. This bit is used to clear the Watchdog Timer and to restart it. This bit is self-clearing, so after the software writes 1 to it the hardware will automatically clear it. If the Watchdog Timer reset is enabled, then the WDCLR has to be set by the user within 512 clocks of the time-out. If this is not done then a Watchdog Timer reset will occur.

15.2 CLOCK CONTROL of Watchdog

WD1, WD0: WDCON.5, WDCON.4 - Watchdog Timer Mode select bits. These two bits select the time-out interval for the watchdog timer. The reset time is 512 clocks longer than the interrupt time-out value.

The default Watchdog time-out is 2^{17} clocks, which is the shortest time-out period. The EWRST, WDIF and WDCLR bits are protected by the Timed Access procedure. This prevents software from accidentally enabling or disabling the watchdog timer. More importantly, it makes it highly improbable that errant code can enable or disable the Watchdog Timer.

The security bit WDTE is located at bit 7 of CONFIG register. This bit is user to configure the clock source of watchdog timer either it is from the internal RC or from the uC clock.

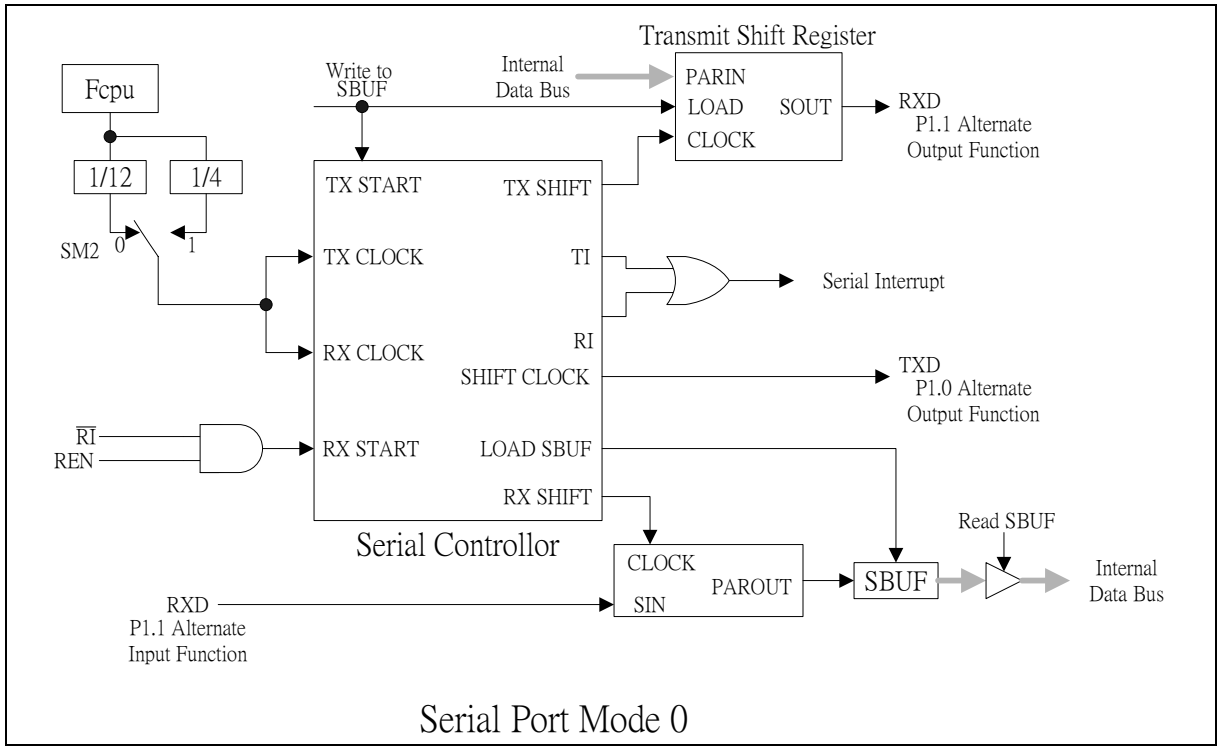
16. SERIAL PORT (UART)

Serial port in the W79E82X series is a full duplex port. The W79E82X series provide the user with additional features such as the Frame Error Detection and the Automatic Address Recognition. The serial ports are capable of synchronous as well as asynchronous communication. In Synchronous mode the W79E82X series generate the clock and operates in a half duplex mode. In the asynchronous mode, full duplex operation is available. This means that it can simultaneously transmit and receive data. The transmit register and the receive buffer are both addressed as SBUF Special Function Register. However any write to SBUF will be to the transmit register, while a read from SBUF will be from the receiver buffer register. The serial port can operate in four different modes as described below.

16.1 MODE 0

This mode provides synchronous communication with external devices. In this mode serial data is transmitted and received on the RXD line. TXD is used to transmit the shift clock. The TxD clock is provided by the W79E82X series whether the device is transmitting or receiving. This mode is therefore a half duplex mode of serial communication. In this mode, 8 bits are transmitted or received per frame. The LSB is Transmitted/Received first. The baud rate is fixed at 1/12 or 1/4 of the oscillator frequency. This Baud Rate is determined by the SM2 bit (SCON.5). When this bit is set to 0, then the serial port runs at 1/12 of the clock. When set to 1, the serial port runs at 1/4 of the clock. This additional facility of programmable baud rate in mode 0 is the only difference between the standard 8051 and the W79E82X series.

The functional block diagram is shown below. Data enters and leaves the Serial port on the RxD line. The TxD line is used to output the shift clock. The shift clock is used to shift data into and out of the W79E82X series and the device at the other end of the line. Any instruction that causes a write to SBUF will start the transmission. The shift clock will be activated and data will be shifted out on the RxD pin till all 8 bits are transmitted. If SM2 = 1, then the data on RxD will appear 1 clock period before the falling edge of shift clock on TxD. The clock on TxD then remains low for 2 clock periods, and then goes high again. If SM2 = 0, the data on RxD will appear 3 clock periods before the falling edge of shift clock on TxD. The clock on TxD then remains low for 6 clock periods, and then goes high again. This ensures that at the receiving end the data on RxD line can either be clocked on the rising edge of the shift clock on TxD or latched when the TxD clock is low.



Serial Port Mode 0

The TI flag is set high in C1 following the end of transmission of the last bit. The serial port will receive data when REN is 1 and RI is zero. The shift clock (TxD) will be activated and the serial port will latch data on the rising edge of shift clock. The external device should therefore present data on the falling edge on the shift clock. This process continues till all the 8 bits have been received. The RI flag is set in C1 following the last rising edge of the shift clock on TxD. This will stop reception, till the RI is cleared by software.

16.2 MODE 1

In Mode 1, the full duplex asynchronous mode is used. Serial communication frames are made up of 10 bits transmitted on TXD and received on RXD. The 10 bits consist of a start bit (0), 8 data bits (LSB first), and a stop bit (1). On received, the stop bit goes into RB8 in the SFR SCON. The baud rate in this mode is variable. The serial baud can be programmed to be 1/16 or 1/32 of the Timer 1 overflow. Since the Timer 1 can be set to different reload values, a wide variation in baud rates is possible.

Transmission begins with a write to SBUF. The serial data is brought out on to TxD pin at C1 following the first roll-over of divide by 16 counter. The next bit is placed on TxD pin at C1 following the next rollover of the divide by 16 counter. Thus the transmission is synchronized to the divide by 16 counter and not directly to the write to SBUF signal. After all 8 bits of data are transmitted, the stop bit is transmitted. The TI flag is set in the C1 state after the stop bit has been put out on TxD pin. This will be at the 10th rollover of the divide by 16 counter after a write to SBUF.

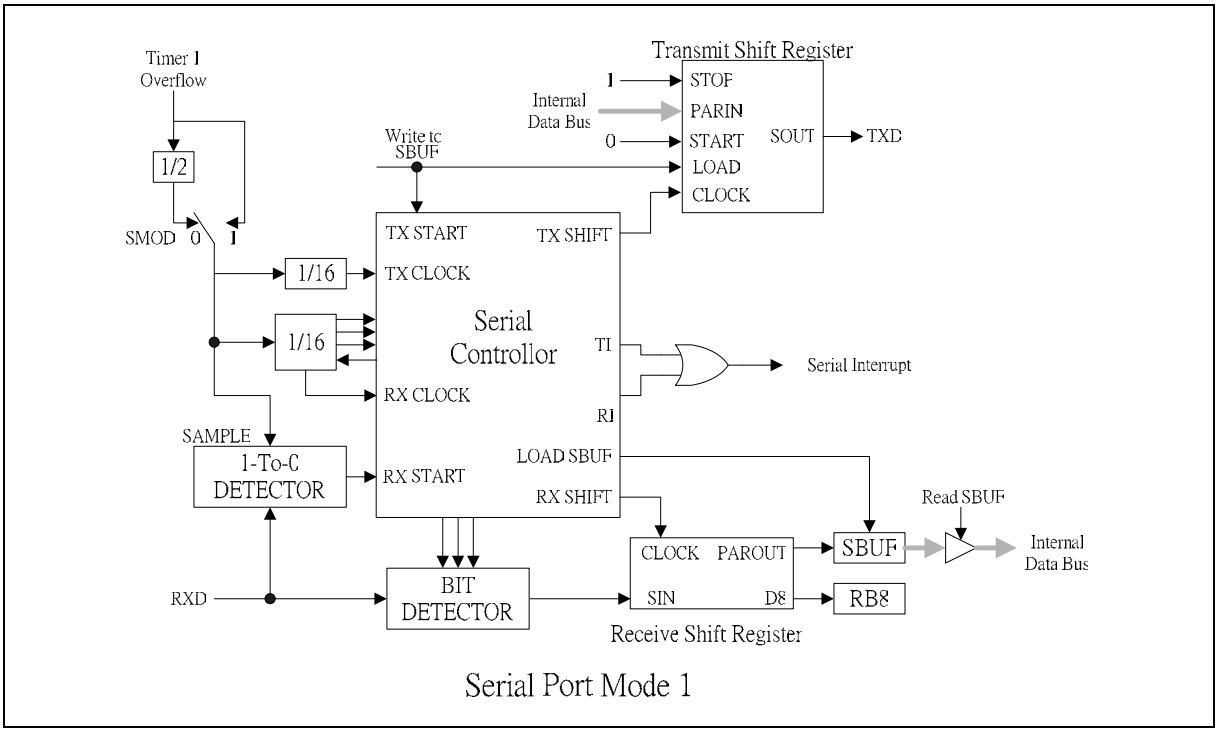
Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of a falling edge on the RxD pin. The 1-to-0 detector continuously monitors the RxD line, sampling it at the rate of 16 times the selected baud rate. When a falling edge is detected, the divide by 16 counter is immediately reset. This helps to align the bit boundaries with the rollovers of the divide by 16 counter.

The 16 states of the counter effectively divide the bit time into 16 slices. The bit detection is done on a best of three basis. The bit detector samples the RxD pin, at the 8th, 9th and 10th counter states. By using a majority 2 of 3 voting system, the bit value is selected. This is done to improve the noise rejection feature of the serial port. If the first bit detected after the falling edge of RxD pin is not 0, then this indicates an invalid start bit, and the reception is immediately aborted. The serial port again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the SBUF.

After shifting in 8 data bits, there is one more shift to do, after which the SBUF and RB8 are loaded and RI is set. However certain conditions must be met before the loading and setting of RI can be done.

1. RI must be 0 and
2. Either SM2 = 0, or the received stop bit = 1.

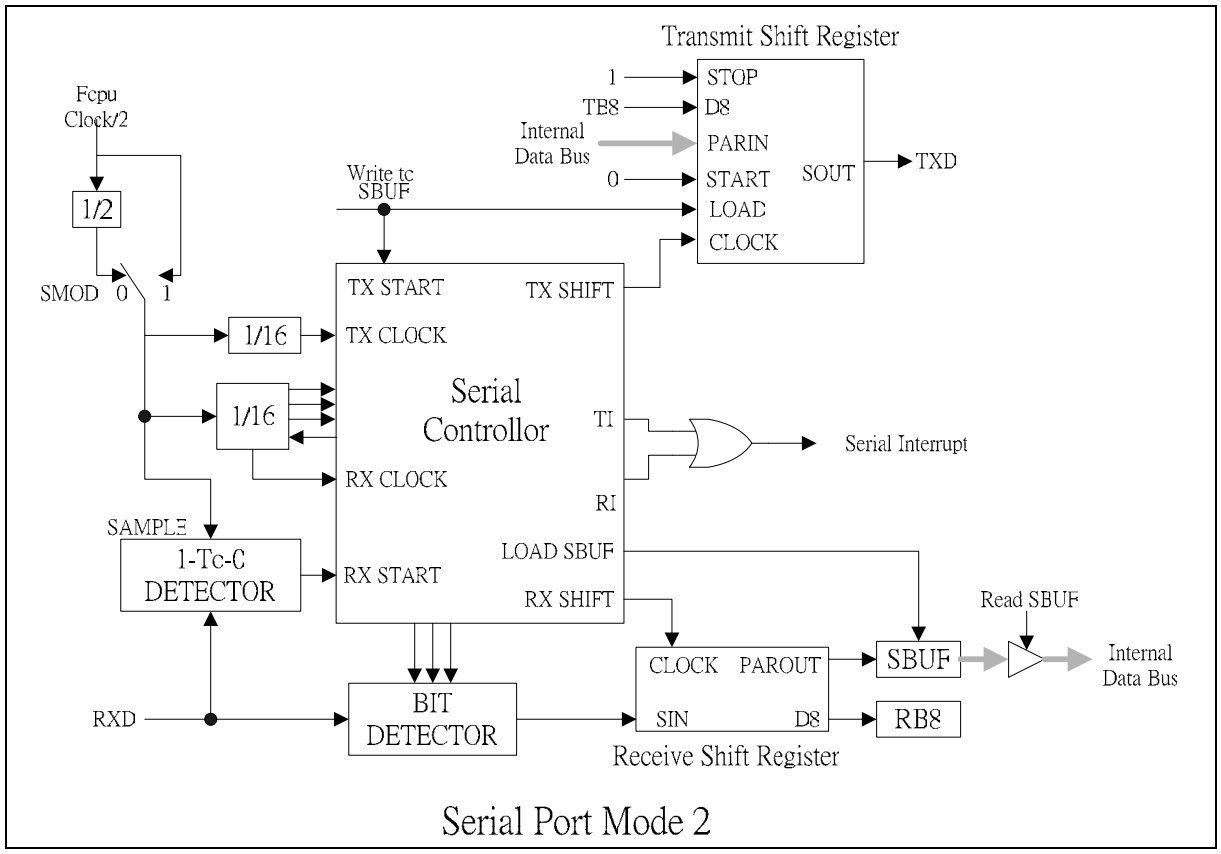
If these conditions are met, then the stop bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost. After the middle of the stop bit, the receiver goes back to looking for a 1-to-0 transition on the RxD pin.



Serial Port Mode 1

16.3 MODE 2

This mode uses a total of 11 bits in asynchronous full-duplex communication. The functional description is shown in the figure below. The frame consists of one start bit (0), 8 data bits (LSB first), a programmable 9th bit (TB8) and a stop bit (0). The 9th bit received is put into RB8. The baud rate is programmable to 1/32 or 1/64 of the oscillator frequency, which is determined by the SMOD bit in PCON SFR. Transmission begins with a write to SBUF. The serial data is brought out on to TxD pin at C1 following the first roll-over of the divide by 16 counter. The next bit is placed on TxD pin at C1 following the next rollover of the divide by 16 counter. Thus the transmission is synchronized to the divide by 16 counter, and not directly to the write to SBUF signal. After all 9 bits of data are transmitted, the stop bit is transmitted. The TI flag is set in the C1 state after the stop bit has been put out on TxD pin. This will be at the 11th rollover of the divide by 16 counter after a write to SBUF. Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of a falling edge on the RxD pin. The 1-to-0 detector continuously monitors the RxD line, sampling it at the rate of 16 times the selected baud rate. When a falling edge is detected, the divide by 16 counter is immediately reset. This helps to align the bit boundaries with the rollovers of the divide by 16 counter. The 16 states of the counter effectively divide the bit time into 16 slices. The bit detection is done on a best of three bases. The bit detector samples the RxD pin, at the 8th, 9th and 10th counter states. By using a majority 2 of 3 voting system, the bit value is selected. This is done to improve the noise rejection feature of the serial port.



Serial Port Mode 2

If the first bit detected after the falling edge of RxD pin, is not 0, then this indicates an invalid start bit, and the reception is immediately aborted. The serial port again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the SBUF. After shifting in 9 data bits, there is one more shift to do, after which the SBUF and RB8 are loaded and RI is set. However certain conditions must be met before the loading and setting of RI can be done.

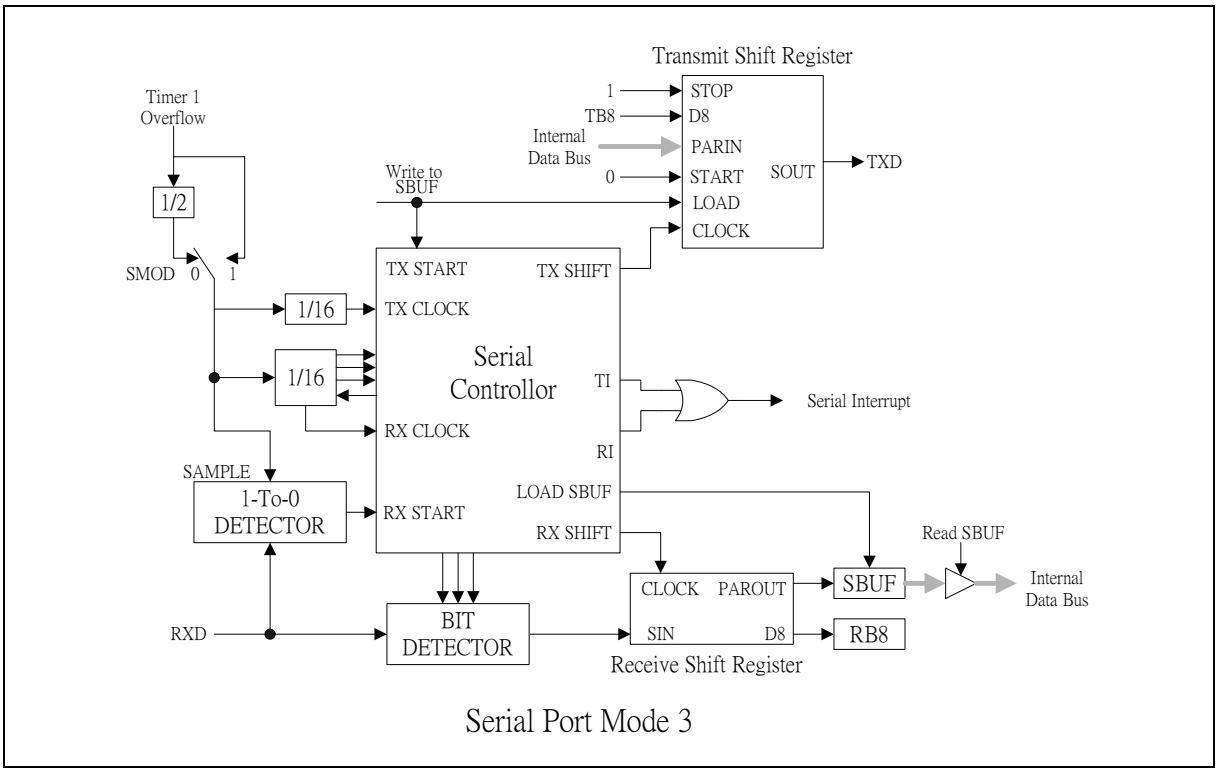
1. RI must be 0 and

2. Either SM2 = 0, or the received stop bit = 1.

If these conditions are met, then the stop bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost. After the middle of the stop bit, the receiver goes back to looking for a 1-to-0 transition on the RxD pin.

16.4 MODE 3

This mode is similar to Mode 2 in all respects, except that the baud rate is programmable. The user must first initialize the Serial related SFR SCON before any communication can take place. This involves selection of the Mode and baud rate. The Timer 1 should also be initialized if modes 1 and 3 are used. In all four modes, transmission is started by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. This will generate a clock on the TxD pin and shift in 8 bits on the RxD pin. Reception is initiated in the other modes by the incoming start bit if REN = 1. The external device will start the communication by transmitting the start bit.



Serial Port Mode 3

Serial Ports Modes

SM0	SM1	MODE	TYPE	BAUD CLOCK	FRAME SIZE	START BIT	STOP BIT	9TH BIT FUNCTION
0	0	0	Synch.	4 or 12 TCLKS	8 bits	No	No	None
0	1	1	Asynch.	Timer 1 or 2	10 bits	1	1	None
1	0	2	Asynch.	32 or 64 TCLKS	11 bits	1	1	0, 1
1	1	3	Asynch.	Timer 1 or 2	11 bits	1	1	0, 1

16.5 Framing Error Detection

A Frame Error occurs when a valid stop bit is not detected. This could indicate incorrect serial data communication. Typically the frame error is due to noise and contention on the serial communication line. The W79E82X series have the facility to detect such framing errors and set a flag which can be checked by software.

The Frame Error FE bit is located in SCON.7. This bit is normally used as SM0 in the standard 8051 family. However, in the W79E82X series it serves a dual function and is called SM0/FE. There are actually two separate flags, one for SM0 and the other for FE. The flag that is actually accessed as SCON.7 is determined by SMOD0 (PCON.6) bit. When SMOD0 is set to 1, then the FE flag is indicated in SM0/FE. When SMOD0 is set to 0, then the SM0 flag is indicated in SM0/FE.

The FE bit is set to 1 by hardware but must be cleared by software. Note that SMOD0 must be 1 while reading or writing to FE. If FE is set, then any following frames received without any error will not clear the FE flag. The clearing has to be done by software.

16.6 Multiprocessor Communications

Multiprocessor communications makes use of the 9th data bit in modes 2 and 3. In the W79E82X series, the RI flag is set only if the received byte corresponds to the Given or Broadcast address. This hardware feature eliminates the software overhead required in checking every received address, and greatly simplifies the software programmer task.

In the multiprocessor communication mode, the address bytes are distinguished from the data bytes by transmitting the address with the 9th bit set high. When the master processor wants to transmit a block of data to one of the slaves, it first sends out the address of the targeted slave (or slaves). All the slave processors should have their SM2 bit set high when waiting for an address byte. This ensures that they will be interrupted only by the reception of a address byte. The Automatic address recognition feature ensures that only the addressed slave will be interrupted. The address comparison is done in hardware not software.

The addressed slave clears the SM2 bit, thereby clearing the way to receive data bytes. With SM2 = 0, the slave will be interrupted on the reception of every single complete frame of data. The unaddressed slaves will be unaffected, as they will be still waiting for their address. In Mode 1, the 9th

bit is the stop bit, which is 1 in case of a valid frame. If SM2 is 1, then RI is set only if a valid frame is received and the received byte matches the Given or Broadcast address.

The Master processor can selectively communicate with groups of slaves by using the Given Address. All the slaves can be addressed together using the Broadcast Address. The addresses for each slave are defined by the SADDR and SADEN SFRs. The slave address is an 8-bit value specified in the SADDR SFR. The SADEN SFR is actually a mask for the byte value in SADDR. If a bit position in SADEN is 0, then the corresponding bit position in SADDR is don't care. Only those bit positions in SADDR whose corresponding bits in SADEN are 1 are used to obtain the Given Address. This gives the user flexibility to address multiple slaves without changing the slave address in SADDR.

The following example shows how the user can define the Given Address to address different slaves.

Slave 1:

SADDR	1010 0100
SADEN	1111 1010
Given	1010 0x0x

Slave 2:

SADDR	1010 0111
SADEN	1111 1001
Given	1010 0xx1

The Given address for slave 1 and 2 differ in the LSB. For slave 1, it is a don't care, while for slave 2 it is 1. Thus to communicate only with slave 1, the master must send an address with LSB = 0 (1010 0000). Similarly the bit 1 position is 0 for slave 1 and don't care for slave 2. Hence to communicate only with slave 2 the master has to transmit an address with bit 1 = 1 (1010 0011). If the master wishes to communicate with both slaves simultaneously, then the address must have bit 0 = 1 and bit 1 = 0. The bit 3 position is don't care for both the slaves. This allows two different addresses to select both slaves (1010 0001 and 1010 0101).

The master can communicate with all the slaves simultaneously with the Broadcast Address. This address is formed from the logical OR of the SADDR and SADEN SFRs. The zeros in the result are defined as don't cares In most cases the Broadcast Address is FFh. In the previous case, the Broadcast Address is (1111111X) for slave 1 and (11111111) for slave 2.

The SADDR and SADEN SFRs are located at address A9h and B9h respectively. On reset, these two SFRs are initialized to 00h. This results in Given Address and Broadcast Address being set as XXXX XXXX(i.e. all bits don't care). This effectively removes the multiprocessor communications feature, since any selectivity is disabled.

17. TIMED ACCESS PROTECTION

The W79E82X series have a new feature, like the Watchdog Timer which is a crucial to proper operation of the system. If left unprotected, errant code may write to the Watchdog control bits resulting in incorrect operation and loss of control. In order to prevent this, the W79E82X series have a protection scheme which controls the write access to critical bits. This protection scheme is done using a timed access.

In this method, the bits which are to be protected have a timed write enable window. A write is successful only if this window is active, otherwise the write will be discarded. This write enable window is open for 3 machine cycles if certain conditions are met. After 3 machine cycles, this window automatically closes. The window is opened by writing AAh and immediately 55h to the Timed Access(TA) SFR. This SFR is located at address C7h. The suggested code for opening the timed access window is

```
TA      REG   0C7h          ;Define new register TA, located at 0C7h
  MOV         TA, #0AAh
  MOV         TA, #055h
```

When the software writes AAh to the TA SFR, a counter is started. This counter waits for 3 machine cycles looking for a write of 55h to TA. If the second write (55h) occurs within 3 machine cycles of the first write (AAh), then the timed access window is opened. It remains open for 3 machine cycles, during which the user may write to the protected bits. Once the window closes the procedure must be repeated to access the other protected bits.

Examples of Timed Assessing are shown below.

Example 1: Valid access

```
  MOV       TA, #0AAh          ;3 M/C     Note: M/C = Machine Cycles
  MOV       TA, #055h          ;3 M/C
  MOV       WDCON, #00h        ;3 M/C
```

Example 2: Valid access

```
  MOV       TA, #0AAh          ;3 M/C
  MOV       TA, #055h          ;3 M/C
  NOP                          ;1 M/C
  SETB      EWRST              ;2 M/C
```

Example 3: Valid access

```
  MOV       TA, #0AAh          ;3 M/C
  MOV       TA, #055h          ;3 M/C
  ORL       WDCON, #00000010B  ;3M/C
```

Example 4: Invalid access

```
MOV     TA, #0AAh       ;3 M/C
MOV     TA, #055h       ;3 M/C
NOP                     ;1 M/C
NOP                     ;1 M/C
CLR     EWT             ;2 M/C
```

Example 5: Invalid Access

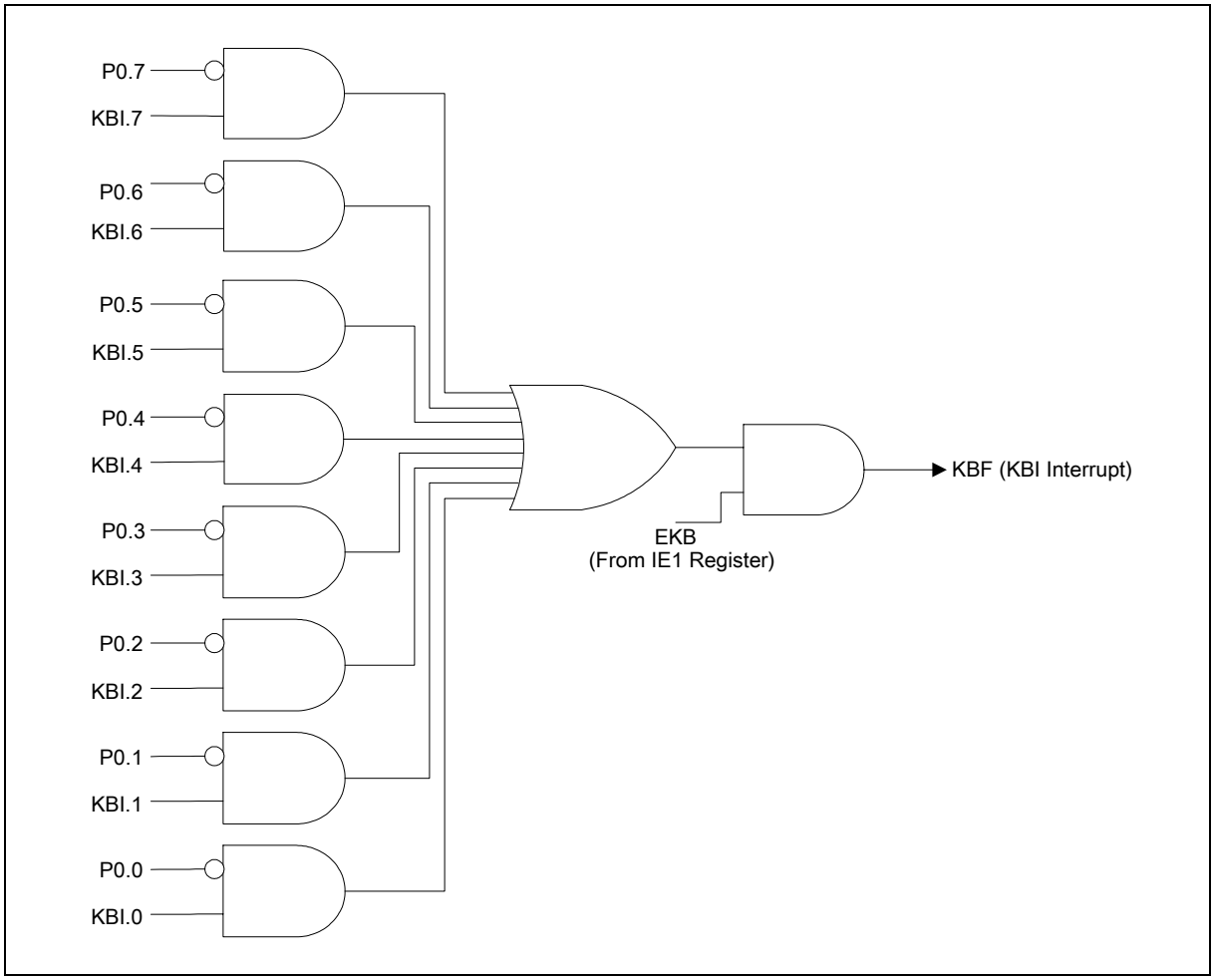
```
MOV     TA, #0AAh       ;3 M/C
NOP                     ;1 M/C
MOV     TA, #055h       ;3 M/C
SETB    EWT             ;2 M/C
```

In the first three examples, the writing to the protected bits is done before the 3 machine cycles window closes. In Example 4, however, the writing to the protected bit occurs after the window has closed, and so there is effectively no change in the status of the protected bit. In Example 5, the second write to TA occurs 4 machine cycles after the first write, therefore the timed access window is not opened at all, and the write to the protected bit fails.

18. KEYBOARD INTERRUPT (KBI)

The W79E82X series are provided 8 keyboard interrupt function to detect keypad status which key is acted, and allow a single interrupt to be generated when any key is pressed on a keyboard or keypad connected to specific pins of the W79E82X series, as shown below Figure. This interrupt may be used to wake up the CPU from Idle or Power Down modes, after chip is in Power Down or Idle Mode.

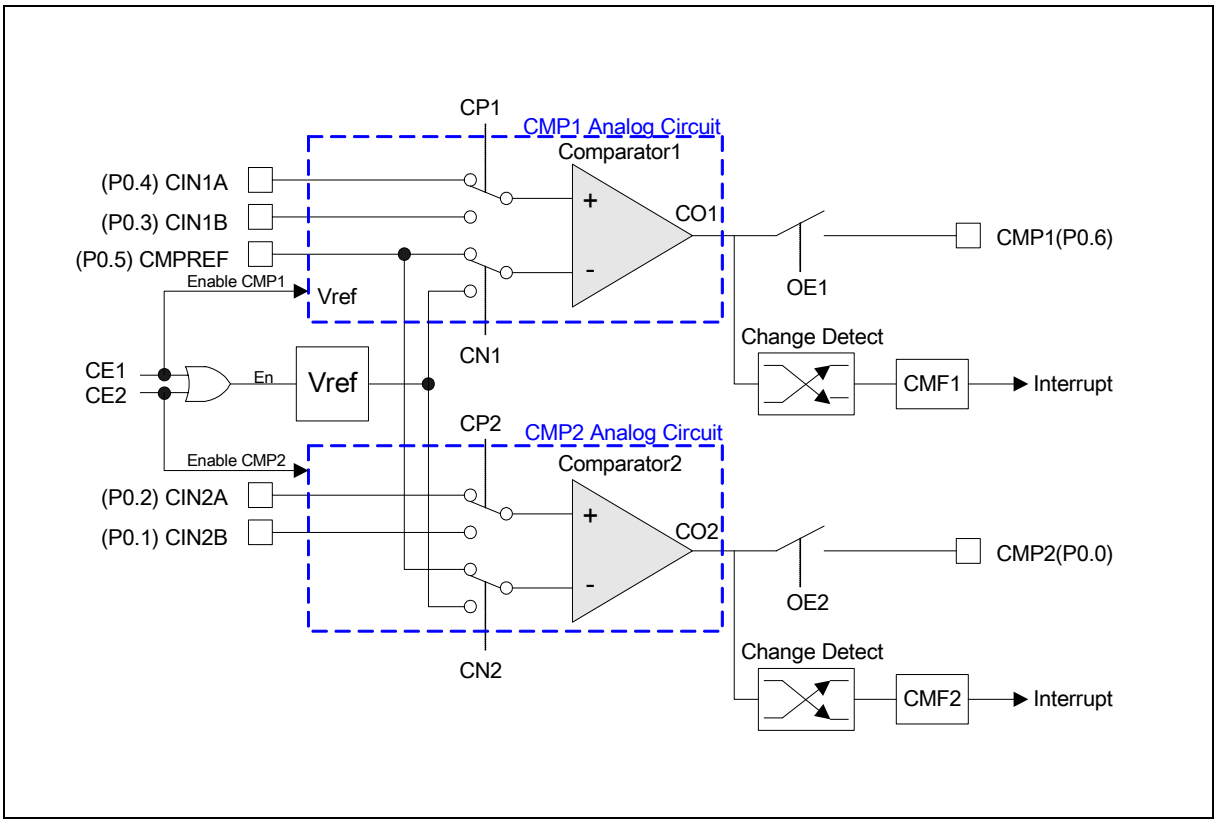
To support keyboard function is by Port 0. It can allow any or all pins of Port 0 to be enabled to cause this interrupt. Port pins are enabled by the setting of bits of KBI0 ~ KBI7 in the KBI register, as shown below Figure. The Keyboard Interrupt Flag (KBF) in the AUXR1 register is set when any enabled pin is pulled low while the KBI interrupt function is active, and the low pulse must more than 1 machine cycle, an interrupt will be generated if it has been enabled. The KBF bit set by hardware and must be cleared by software. In order to determine which key was pressed, the KBI will allow the interrupt service routine to poll port 0.



19. ANALOG COMPARATORS

The W79E82X series are provided two Comparators. Input and output options allow use of the comparators in a number of different Configurations. The Comparator output is a logical one when its positive input is greater than its negative input, otherwise the output is a zero. Each Comparator can be configured to cause to an interrupt when the output value change. The block diagram is as below.

Each Comparator has a control register (CMP1 and CMP2), Both Inputs are CINnA, CINnB, CMPREF and internal reference voltage, and outputs are CMP1 and CMP2 by setting OEn bit. After enable Comparators the Comparator need waited stable time to guarantee Comparator output. If programmer used internal reference voltage, it will be set OEn bit to "1". The value of internal reference voltage (Vref) is 1.19V +/- 10%.



20. I/O PORT CONFIGURATION

The W79E82X series have three I/O ports, port 0, port 1 and port 2. All pins of I/O ports can be configured to one of four types by software except P1.5 is only input pin. When P1.5 is configured reset pin by RPD=0 in the CONFIG 1 register, the W79E82X series can support 15 pins by use Crystal. If used on-chip RC oscillator the P1.5 is configured input pin, the W79E82X series can be supported up to 18 pins. The I/O ports configuration setting as below table.

I/O port configuration table

PXM1.Y	PXM2.Y	PORT INPUT/OUTPUT MODE
0	0	Quasi-bidirectional
0	1	Push-Pull
1	0	Input Only (High Impedance) P2M1.PxS=0, TTL input P2M1.PxS=1, Schmitt input
1	1	Open Drain

All port pins can be determined to high or low after reset by configure PRHI bit in the CONFIG1 register. After reset, these pins are in quasi-bidirectional mode. The port pin of P1.5 only is a Schmitt trigger input.

Enabled toggle outputs from Timer 0 and Timer 1 by ENT0 and ENT1 on P2M1 register, the output frequency of Timer 0 or Timer 1 is by Timer overflow.

Each I/O port of the W79E82X series may be selected to use TTL level inputs or Schmitt inputs by P(n)S bit on P2M1 register, where n is 0, 1 or 2. When P(n)S is set to 1, Ports are selected Schmitt trigger inputs on Port(n). The P2.0(XTAL2) can be configured clock output when used on-chip RC or external Oscillator is clock source, and the frequency of clock output is divided by 4 on on-chip RC clock or external Oscillator.

20.1 Quasi-Bidirectional Output Configuration

After chip was power on or reset, the all ports output are this mode, and output is common with the 8051. This mode can be used as both an input and output without the need to reconfigure the port.

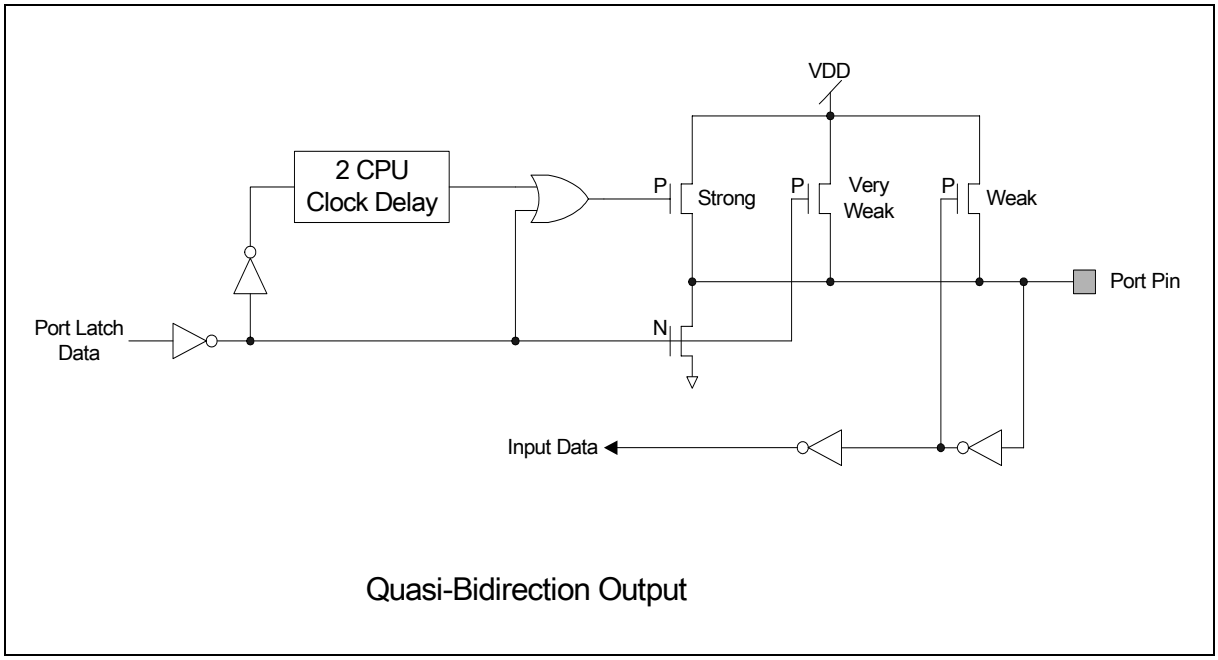
When the pin is pulled low, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

This mode has three pull-up resisters that are “strong” pull-up, “weak” pull-up and “very weak” pull-up. The “strong” pull-up is used fast transition from logic “0” change to logic “1”, and it is fast latch and transition. When port pins is occur from logic “0” to logic “1”, the strong pull-up will quickly turn on two CPU clocks to pull high then turn off.

The “weak” pull-up is turned on when the input port pin is logic “1” level or itself is logic “1”, and it provides the most source current for a quasi-bidirectional pin that output is “1” or port latch is logic “0”’.

The “very weak” pull-up is turned on when the port latch is logic “1”. If port latch is logic “0”, it will be turned off. The very weak pull-up is support a very small current that will pull the pin high if it is left floating. And the quasi-bidirectional port configuration is shown as below figure.

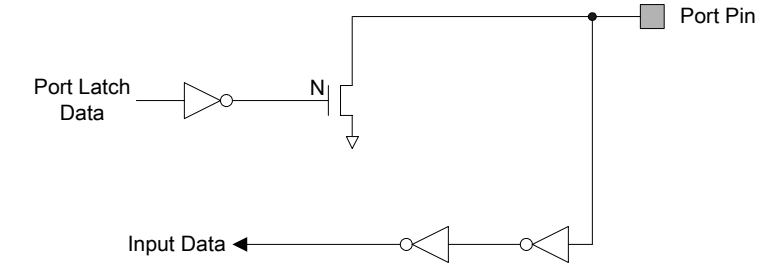
If port pin is low, it can drives large sink current for output, and it is similar with push-pull and open drain on sink current output.



Quasi-Bidirection Output

20.2 Open Drain Output Configuration

To configure this mode is turned off all pull-ups. If used similar as a logic output, the port must has an external pull-up resister. The open drain port configuration is shown as below.

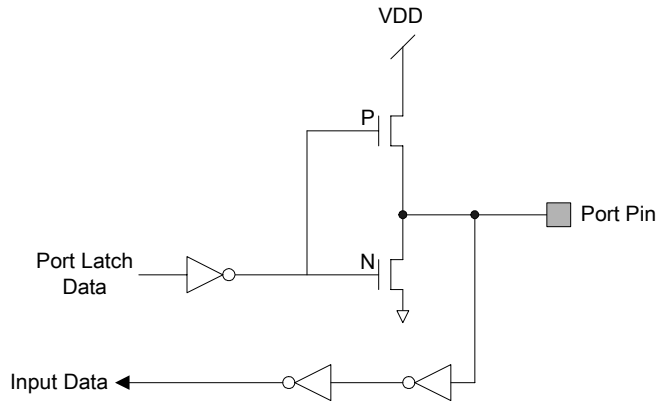


Open Drain Output

20.3 Push-Pull Output Configuration

The push-pull output mode has two strong pull-up and pull-down structure that support large source and sink current output. it remove “weak” pull-up and “very weak” pull-up resister and remain “strong pull-up resister on quasi-bidirectional output mode. The “strong” pull-up is always turns on when port latch is logic “1” to support source current. The push-pull port configuration is shown in below Figure.

The W79E82X series have three port pins that can’t be configured are P1.2, P1.3, and P1.5. The port pins P1.2 and P1.3 are configured to open drain outputs. They may be used as inputs by writing ones to their respective port latches.



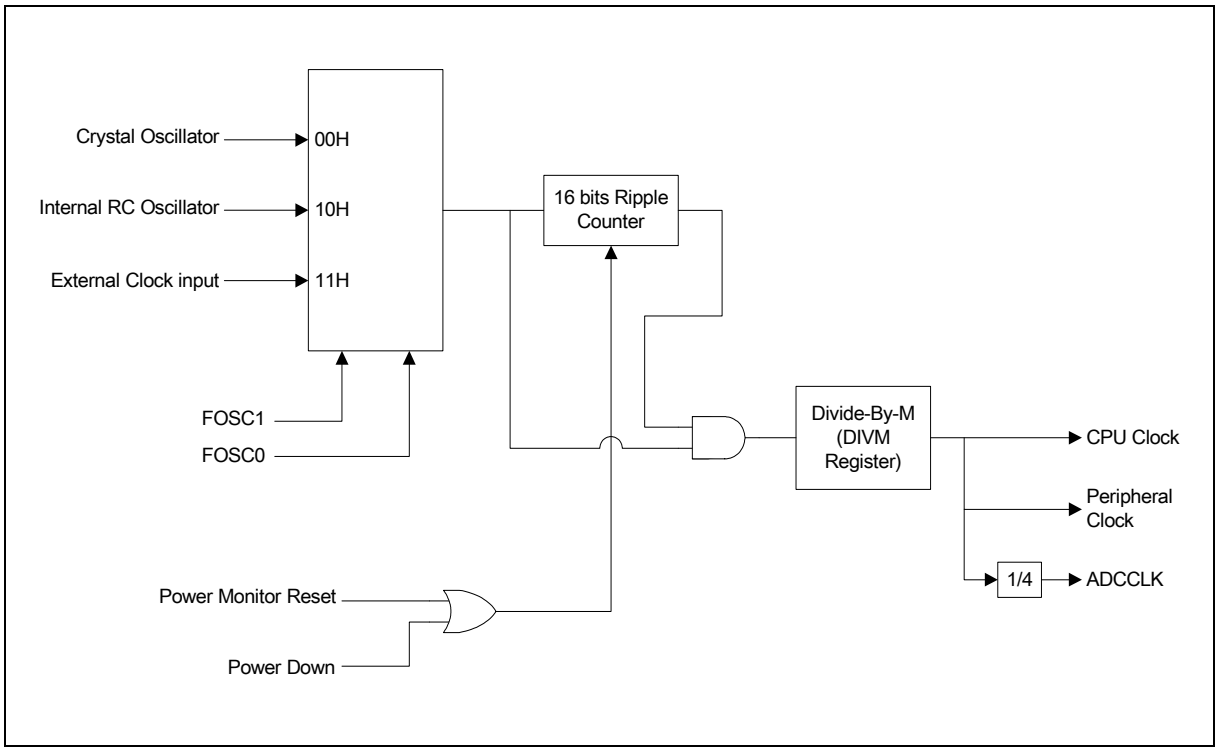
Push-Pull Output

20.4 Input Only Configuration

By configure this mode, the ports are only digital input and disable digital output. The W79E82X series can select input pin to Schmitt trigger or TTL level input by PxM1.y and PxM2.y registers.

21. OSCILLATOR

The W79E82X series provides three oscillator input option. These are configured at CONFIG register (CONFIG1) that include On-Chip RC Oscillator Option, External Clock Input Option and Crystal Oscillator Input Option. The Crystal Oscillator Input frequency may be supported from 4MHz to 20MHz, and without capacitor or resister.



21.1 On-Chip RC Oscillator Option

The On-Chip RC Oscillator is fixed at 6MHz +/- 25% frequency to support clock source. When FOSC1, FOSC0 = 10H, the On-Chip RC Oscillator is enabled. A clock output on P2.0 (XTAL2) may be enabled when On-Chip RC oscillator is used.

21.2 External Clock Input Option

The clock source pin (XTAL1) is from External Clock Input by FOSC1, FOSC0 = 11H, and frequency range is form 0Hz up to 20MHz. A clock output on P2.0 (XTAL2) may be enabled when External Clock Input is used.

The W79E82X series supports a clock output function when either the on-chip RC oscillator or the external clock input options is selected. This allows external devices to synchronize to the W79E82X serial. When enabled, via the ENCLK bit in the P2M1 register, the clock output appears on the XTAL2/CLKOUT pin whenever the on-chip oscillator is running, including in Idle Mode. The frequency of the clock output is 1/4 of the CPU clock rate. If the clock output is not needed in Idle Mode, it may be turned off prior to entering Idle mode, saving additional power. The clock output may also be enabled when the external clock input option is selected.

21.3 CPU Clock Rate select

The CPU clock of W79E82X series may be selected by the DIVM register. If DIVM = 00H, the CPU clock is running at 4 CPU clock pre machine cycle, and without any division from source clock (Fosc). When the DIVM register is set to N value, the CPU clock is divided by 2(DVIM+1), so CPU clock frequency division is from 4 to 512. The user may use this feature to set CPU at a lower speed rate for reducing power consumption. This is very similar to the situation when CPU has entered Idle mode. In addition this frequency division function affect all peripheral timings as they are all sourcing from the CPU clock(Fcpu).

22. POWER MONITORING FUNCTION

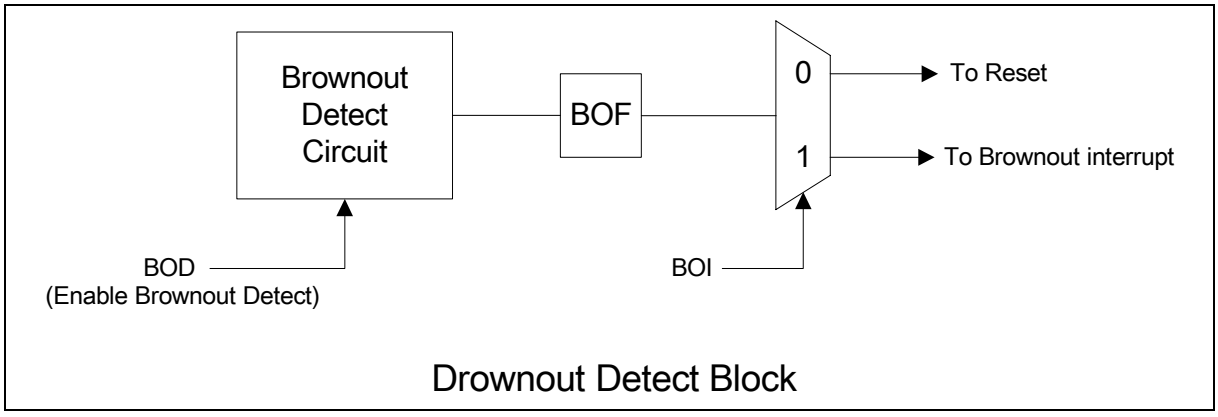
Power-On Detect and Brownout are two additional power monitoring functions implemented in W79E82X to prevent incorrect operation during power up and power drop or loss.

22.1 Power On Detect

The Power–On Detect function is a designed to detect power up after power voltage reaches to a level where Brownout Detect can work. After power on detect, the POR (PCON.4) will be set to “1” to indicate an initial power up condition. The POR flag will be cleared by software.

22.2 Brownout Detect

The Brownout Detect function is detect power voltage is drops to brownout voltage level, and allows preventing some process work or indicate power warming. The W79E82X series have two brownout voltage levels to select by BOV (CONFIG1.4). If BOV =0 that brownout voltage level is 3.8V, If BOV = 1 that brownout voltage level is 2.5V. When the Brownout voltage is drop to select level, the brownout detector will detect and keeps this active until VDD is returns to above brownout Detect voltage. The Brownout Detect block is as follow.



Drownout Detect Block

When Brownout Detect is enabled by BOD (AUXR1.6), the BOF (PCON.5) flag will be set that it cause brownout reset or interrupt, and BOF will be cleared by software. If BOI (AUXR1.5) is set to “1”, the brownout detect will cause interrupt via the EA (IE.7) and EBO (IE.5) bits is set.

In order to guarantee a correct detection of Brownout, The VDD fail time must be slower than 50mV/us, and rise time is slower than 2mV/us to ensure a proper reset.

23. PULSE WIDTH MODULATED OUTPUTS (PWM)

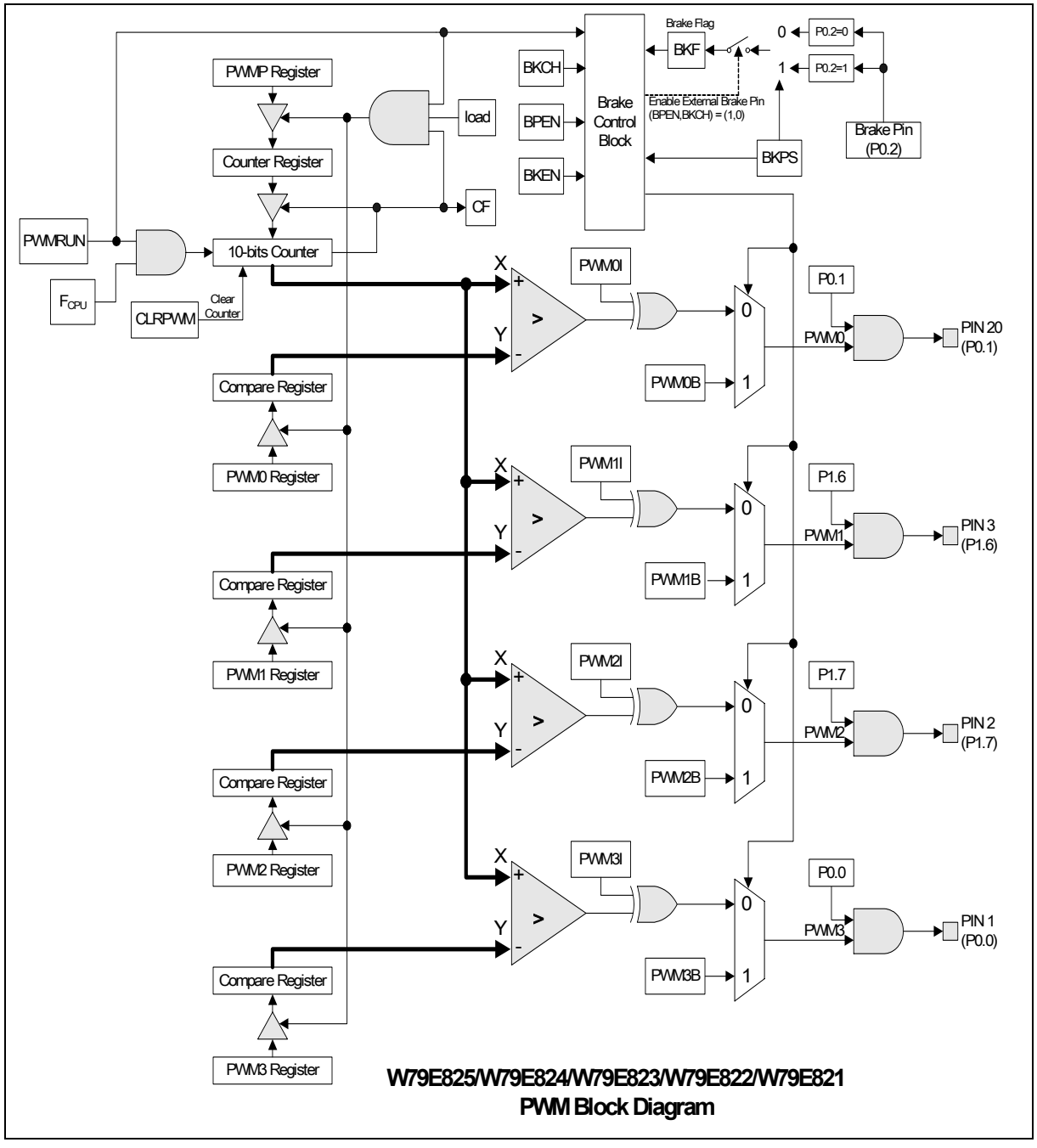
The W79E82X series have four-channels Pulse Width Modulated (PWM), and the PWM outputs are PWM0(P0.1), PWM1(P1.6), PWM2(P1.7) and PWM3(P0.0). When PRHI is set to “1”, after chip reset, the internal output of the each PWM channels are “1”. When PRHI is set to “0”, after chip reset, the internal output of the each PWM channels are “0”. So, in the case, if PWM output pins will output “1”, it must be written a “1” to each PWM pins to high state. A block diagram is shown as below Figure.

The W79E82X series support 10-bits down counter which clock source of counter is use the internal microcontroller clock as its input. The PWM counter clock, has the same frequency as the clock source F_{CPU} = F_{OSC}. When the counter reaches underflow it will automatic reloaded from counter register. The PWM frequency is given by: f_{PWM} = F_{CPU} / (PWMP+1), where PWMP is 10-bits register of PWMPH.1, PWMPH.0 and PWMPL.7~PWMPL.0.

When PWMP register is written, it will automatically load by PWMRUN, Load and CF is “1”, where CF flag is 10-bits down counter reaches underflow, the CF flag will be cleared by software. When PWMP register was load to counter register, the load bit will automatically clear by next cycle. If the first PWM output cycle is correct by PWMP setting, it will be clear by CLRPWM to clear 10-bits counter to 000H, then set PWMRUN and load bits to run PWM.

The pulse width of each PWM output is determined by the Compare registers of PWM0L through PWM3L and PWM0H through PWM3H. When PWM compare register is greater than 10-bits counter register, the PWM output is low. If want to change output width of PWM, after writer PWMn register, must set load bit to “1” then will be loaded to compare register by next underflow. The PWM output high pulses width is given by:

t_{HI} = (PWMP – PWMn+1). Notice, if compare register is set to 000H, the PWMn output is high, and if compare register is set to 3FFH, the PWMn output is low.



W79E825/W79E824/W79E823/W79E822/W79E821
PWM Block Diagram

The all PWM control registers are PWMCON1, PWMCON2, and PWMCON3 register, and function description as below.

PWM Counter Low Bits Register PWMPL(D9H)

BIT	NAME	FUNCTION
7~0	PWMP.7 ~PWMP.0	PWM Counter low bit 7~0 register

PWM Counter High Bits Register PWMPH(D1H)

BIT	NAME	FUNCTION
7~2	-	Reserved
1~0	PWMP.9 ~PWMP.8	PWM Counter high bit 9~8 register

PWM 0 Low Bits Register PWM0L(DAH)

BIT	NAME	FUNCTION
7~0	PWM0.7 ~PWM0.0	PWM 0 low bit 7~0 register

PWM 1 Low Bits Register PWM1L(DBH)

BIT	NAME	FUNCTION
7~0	PWM1.7 ~PWM1.0	PWM 1 low bit 7~0 register

PWM 2 Low Bits Register PWM2L(DDH)

BIT	NAME	FUNCTION
7~0	PWM2.7 ~PWM2.0	PWM 2 low bit 7~0 register

PWM 3 Low Bits Register PWM3L(DEH)

BIT	NAME	FUNCTION
7~0	PWM3.7 ~PWM3.0	PWM3 low bit 7~0 register

PWM 0 High Bits Register PWM0H(D2H)

BIT	NAME	FUNCTION
7~2	-	Reserved
1~0	PWM0.9 ~PWM0.8	PWM 0 high bit 9~8 register

PWM 1 High Bits Register PWM1H(D3H)

BIT	NAME	FUNCTION
7~2	-	Reserved
1~0	PWM1.9 ~PWM1.8	PWM 1 high bit 9~8 register

PWM 2 High Bits Register PWM2H(D5H)

BIT	NAME	FUNCTION
7~2	-	Reserved
1~0	PWM2.9 ~PWM2.8	PWM 2 high bit 9~8 register

PWM 3 High Bits Register PWM3H(D6H)

BIT	NAME	FUNCTION
7~2	-	Reserved
1~0	PWM3.9 ~PWM3.8	PWM 3 high bit 9~8 register

PWM Control Register 1 PWMCON1(DCH)

BIT	NAME	FUNCTION
7	PWMRUN	0: The PWM is not running. 1: The PWM counter is running.
6	load	0: The registers value of PWMP and PWMn is without loaded to counter and compare registers. 1: The PWMP and PWMn registers load value to counter and compare registers at the counter underflow. This bit is automatically cleared by hardware after the PWMP and PWMn are transferred to counter and compare register.
5	CF	10-bit counter overflow flag: 0: The 10-bit counter down count is not overflow. 1: The 10-bit counter down count is overflow. It will be cleared by software.
4	CLRPWM	1: Clear 10-bit PWM counter to 000H. The bit will automatically cleared by next cycle.

Continued

BIT	NAME	FUNCTION
3	PWM3I	0: PWM3 out is non-inverted. 1: PWM3 output is inverted.
2	PWM2I	0: PWM2 out is non-inverted. 1: PWM2 output is inverted.
1	PWM1I	0: PWM1 out is non-inverted. 1: PWM1 output is inverted.
0	PWM0I	0: PWM0 out is non-inverted. 1: PWM0 output is inverted.

PWM Control Register 2 PWMCON2(DFH)

BIT	NAME	FUNCTION
7	BKCH	See the below table, when BKEN is set.
6	BKPS	0: Brake is asserted if P0.2 is low. 1: Brake is asserted if P0.2 is high
5	BPEN	See the below table, when BKEN is set.
4	BKEN	0: The Brake is never asserted. 1: The Brake is enabled, and see the below table.
3	PWM3B	0: The PWM3 output is low, when Brake is asserted. 1: The PWM3 output is high, when Brake is asserted.
2	PWM2B	0: The PWM2 output is low, when Brake is asserted. 1: The PWM2 output is high, when Brake is asserted.
1	PWM1B	0: The PWM1 output is low, when Brake is asserted. 1: The PWM1 output is high, when Brake is asserted.
0	PWM0B	0: The PWM0 output is low, when Brake is asserted. 1: The PWM0 output is high, when Brake is asserted.

Brake Condition table

BPEN	BKCH	BREAK CONDITION
0	0	Brake On, Software Brake
0	1	On, when PWM is not running, the PWM output condition is follow PWMnB setting.
1	0	On, when Brake pin asserted, no PWM output, the BKF will be set and PWMRUN will be cleared.
1	1	No any active.

PWM Control Register 3 PWMCON3(D7H)

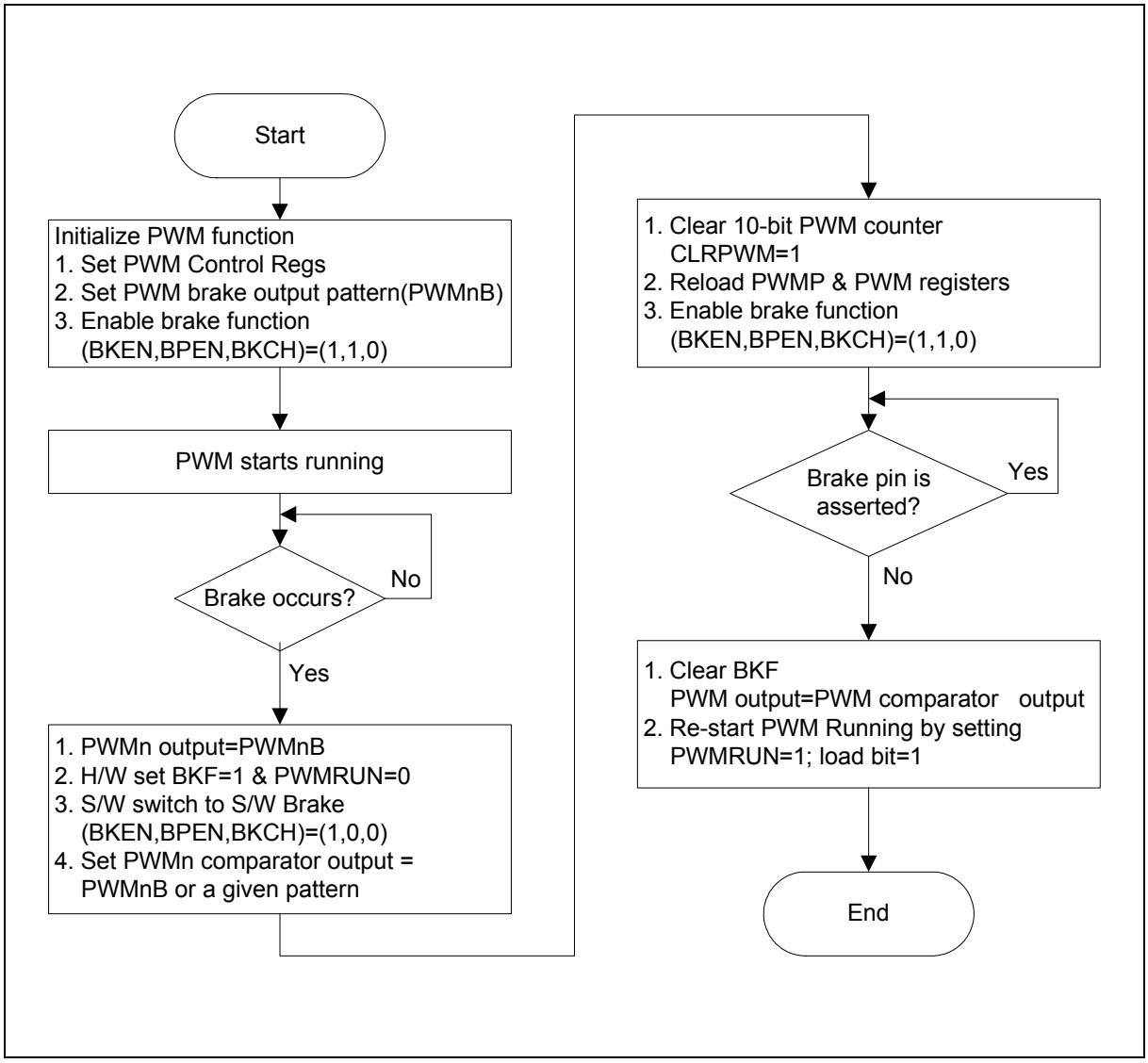
BIT	NAME	FUNCTION
7~1	-	Reserved
0	BKF	The external brake pin flag. 0: The PWM is not brake. 1: The PWM is brake by external brake pin. It will be cleared by software. If this bit is set, PWMRUN can't be set.

The W79E82X series chips have support brake function by software or external pin(P0.2). That brake control is by PWMCON2 register. The software brake and external pin brake setting as refer brake condition table. When brake is asserted, the PWM outputs are by PWMnB setting. By the software brake, the BKEN is set to "1" that will enable brake function and determined by BPEN and BKCH bits. The (BPEN, BKCH) = (0,0), brake is asserted. The (BPEN, BKCH) = (0,1), the PWM outputs are follow PWMRUN bit; When PWM is not running that mean is PWMRUN = 0, the PWM outputs are asserted by PWMnB setting; When PWM is running, the PWMRUN = 1, and keeping PWM outputs.

By the external brake pin(P0.2) brake, W79E82X series chips have brake interrupt service or polling brake flag (BKF) if external pin is asserted. If to decide P0.2 is low is asserted by BKPS = 0, the BKF(PWMCON3.0) will be set to "1" and PWNRUN will be cleared to stop PWM run, the PWM outputs condition are by PWMnB setting. After brake pin is release,

Since the Brake Pin being asserted will automatically clear the Run bit and BKF(PWMCON3.0) flag will be set, PWMCON1.7, the user program can poll this bit or enable PWM's brake interrupt to determine when the Brake Pin causes a brake to occur. The other method for detecting a brake caused by the Brake Pin would be to tie the Brake Pin to one of the external interrupt pins. This latter approach is needed if the Brake signal can be of insufficient length to ensure that it can be captured by a polling routine. When, after being asserted, the condition causing the brake is removed, the PWM outputs go to whatever state that had immediately prior to the brake. This means that in order to go from brake being asserted to having the PWM run without going through an indeterminate state care must be taken. If the

In order to smoothly release brake by external brake pin is asserted then PWM is going to run, the step interval as refer below figure.


Start
Initialize PWM function
1. Set PWM Control Regs
2. Set PWM brake output pattern(PWMnB)
3. Enable brake function
(BKEN,BPEN,BKCH)=(1,1,0)
PWM starts running
Brake occurs?
No
Yes
1. PWMn output=PWMnB
2. H/W set BKF=1 & PWMRUN=0
3. S/W switch to S/W Brake
(BKEN,BPEN,BKCH)=(1,0,0)
4. Set PWMn comparator output =
PWMnB or a given pattern
1. Clear 10-bit PWM counter
CLRPWM=1
2. Reload PWMP & PWM registers
3. Enable brake function
(BKEN,BPEN,BKCH)=(1,1,0)
Brake pin is asserted?
Yes
No
1. Clear BKF
PWM output=PWM comparator output
2. Re-start PWM Running by setting
PWMRUN=1; load bit=1
End

24. ANALOG-TO-DIGITAL CONVERTER

The ADC contains a DAC which converts the contents of a successive approximation register to a voltage (VDAC) which is compared to the analog input voltage (Vin). The output of the comparator is fed to the successive approximation control logic which controls the successive approximation register. A conversion is initiated by setting ADCS in the ADCCON register. ADCS can be set by software only or by either hardware or software.

The software only start mode is selected when control bit ADCCON.5 (ADCEX) =0. A conversion is then started by setting control bit ADCCON.3 (ADCS) The hardware or software start mode is selected when ADCCON.5 =1, and a conversion may be started by setting ADCCON.3 as above or by applying a rising edge to external pin STADC. When a conversion is started by applying a rising edge, a low level must be applied to STADC for at least one machine cycle followed by a high level for at least one machine cycle.

The low-to-high transition of STADC is recognized at the end of a machine cycle, and the conversion commences at the beginning of the next cycle. When a conversion is initiated by software, the conversion starts at the beginning of the machine cycle which follows the instruction that sets ADCS. ADCS is actually implemented with tpw flip-flops: a command flip-flop which is affected by set operations, and a status flag which is accessed during read operations.

The next two machine cycles are used to initiate the converter. At the end of the first cycle, the ADCS status flag is set end a value of “1” will be returned if the ADCS flag is read while the conversion is in progress. Sampling of the analog input commences at the end of the second cycle.

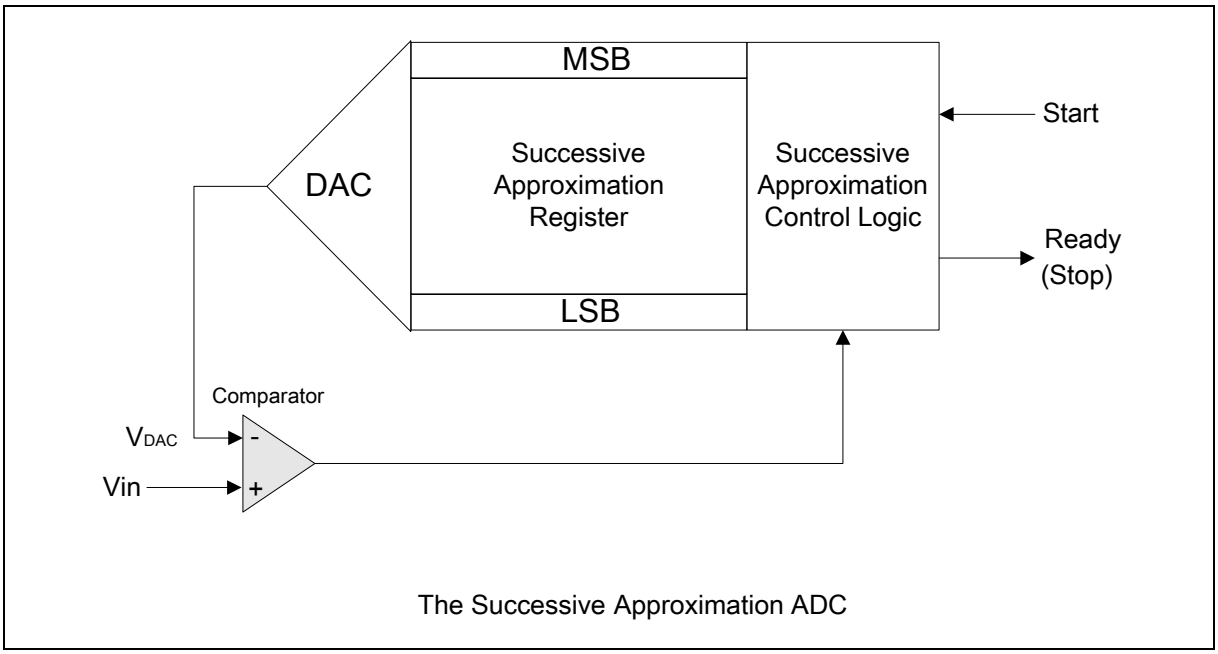
During the next eight machine cycles, the voltage at the previously selected pin of one of analog input pin is sampled, and this input voltage should be stable in order to obtain a useful sample. In any event, the input voltage slew rate must be less than 10V/ms in order to prevent an undefined result.

The successive approximation control logic first sets the most significant bit and clears all other bits in the successive approximation register (10 0000 0000b). The output of the DAC (50% full scale) is compared to the input voltage Vin. If the input voltage is greater than VDAC, then the bit remains set; otherwise if is cleared.

The successive approximation control logic now sets the next most significant bit (11 0000 0000b or 01 0000 0000b, depending on the previous result), and the VDAC is compared to Vin again. If the input voltage is greater then VDAC, then the bit remains set; otherwise it is cleared. This process is repeated until all ten bits have been tested, at which stage the result of the conversion is held in the successive approximation register. The conversion takes four machine cycles per bit.

The end of the 10-bit conversion is flagged by control bit ADCCON.4 (ADCI). The upper 8 bits of the result are held in special function register ADCH, and the two remaining bits are held in ADCCON.7 (ADC.1) and ADCCON.6 (ADC.0). The user may ignore the two least significant bits in ADCCON and use the ADC as an 8-bit converter (8 upper bits in ADCH). In any event, the total actual conversion time is 52 machine cycles. ADCI will be set and the ADCS status flag will be reset 52 cycles after the ADCS is set. Control bits ADCCON.0 and ADCCON.1 are used to control an analog multiplexer which

selects one of 4 analog channels. An ADC conversion in progress is unaffected by an external or software ADC start. The result of a completed conversion remains unaffected provided ADCI = logic 1; a new ADC conversion already in progress is aborted when the idle or power down mode is entered. The result of a completed conversion (ADCI = logic 1) remains unaffected when entering the idle mode.



Successive Approximation ADC

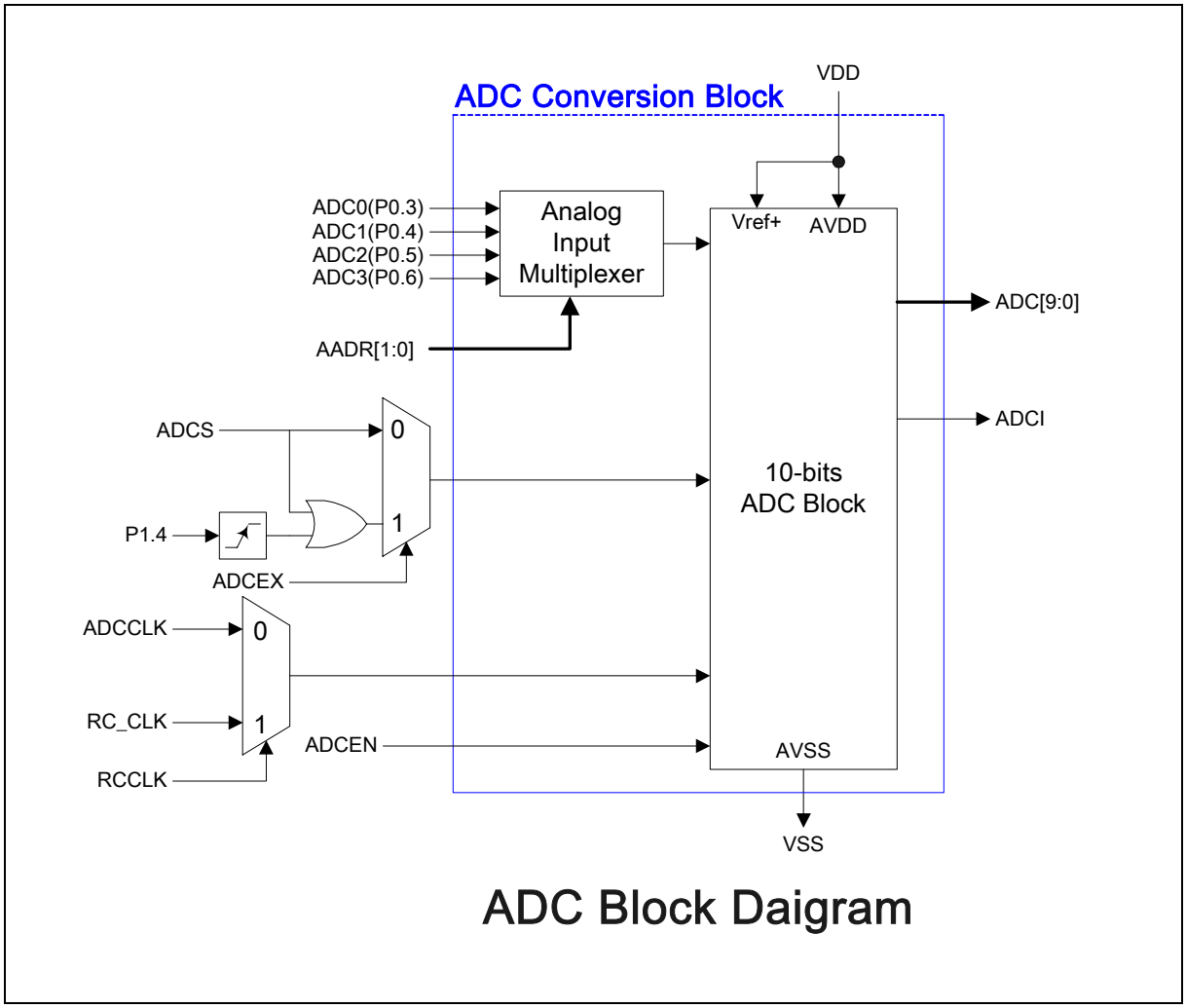
24.1 ADC Resolution and Analog Supply:

The ADC circuit has its own supply pins (AVDD and AVSS) and one pins (Vref+) connected to each end of the DAC's resistance-ladder that the AVDD and Vref+ are connected to VDD and AVSS is connected to VSS. The ladder has 1023 equally spaced taps, separated by a resistance of "R". The first tap is located 0.5×R above AVSS, and the last tap is located 0.5×R below Vref+. This gives a total ladder resistance of 1024×R. This structure ensures that the DAC is monotonic and results in a symmetrical quantization error.

For input voltages between VSS and [(Vref+) + ½ LSB], the 10-bit result of an A/D conversion will be 0000000000B = 000H. For input voltages between [(Vref+) – 3/2 LSB] and Vref+, the result of a conversion will be 1111111111B = 3FFH. Vref+ and AVSS may be between AVDD + 0.2V and VSS – 0.2 V. Vref+ should be positive with respect to VSS, and the input voltage (Vin) should be between Vref+ and VSS.

The result can always be calculated from the following formula:

$$\text{Result} = 1024 \times \frac{\text{Vin}}{\text{Vref}+} \quad \text{or Result} = 1024 \times \frac{\text{Vin}}{\text{VDD}}$$



The ADC Block Diagram

25. I2C SERIAL CONTROL

The I2C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the bus are:

– Bidirectional data transfer between masters and slaves

– Multimaster bus (no central master)

– Arbitration between simultaneously transmitting masters without corruption of serial data on the bus

– Serial clock synchronization allows devices with different bit rates to communicate via one serial bus

– Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer

– The I2C bus may be used for test and diagnostic purposes

The output latches of P1.2 and P1.3 must be set to logic 1 in order to enable SIO1.

The W79E82X series on-chip I2C logic provide a serial interface that meets the I2C bus specification and supports all transfer modes (other than the low-speed mode) from and to the I2C bus. The I2C logic handles bytes transfer autonomously. It also keeps track of serial transfers, via a status register (I2STATUS) which reflects the status of the I2C bus.

The CPU interfaces to the I2C logic via the following four special function registers: I2CON (SIO1 control register), I2STATUS (SIO1 status register), I2DAT (SIO1 data register), and I2ADR (SIO1 slave address register). The SIO1 logic interfaces to the external I2C bus via two port 1 pins: P1.2/SCL (serial clock line) and P1.3/SDA (serial data line).

25.1 SIO1 Port

The SIO1 port is a serial I/O port, which supports all transfer modes from and to the I2C bus. The SIO1 port handles byte transfers autonomously. To enable this port, the bit ENS1 in I2CON should be set to '1'. The CPU interfaces to the SIO1 port through the following six special function registers: **I2CON** (control register, C0H), **I2STATUS** (status register, BDH), **I2DAT** (data register, BCH), **I2ADDR** (address registers, C1H), **I2CLK** (clock rate register BEH) and **I2TIMER** (Timer counter register, BFH). The SIO1 H/W interfaces to the I2C bus via two pins: SDA (P1.3, serial data line) and SCL (P1.2, serial clock line). The output latches of P1.2 and P1.3 must be set to "1" before using this port.

25.2 The I2C Control Registers:

The W79E82X series need set some control registers to control I2C serial port. Please reference detail description is shown below.

25.2.1 The Address Registers, I2ADDR

The SIO1 is equipped with a address registers: I2ADDR. The CPU can read from and write to an 8-bit, directly addressable SFRs. The content of these registers are irrelevant when SIO1 is in master modes. In the slave modes, the seven most significant bits must be loaded with the MCU's own address. The SIO1 hardware will react if either of the addresses is matched.

When GC bit is set, the I2C is in Slave mode, it can be received the general call address by 00H after Master send general call address to I2C bus, then it will follow status of GC mode. If it is in Master mode, the AA bit must be cleared when it will send general call address of 00H to I2C bus.

Bit:	7	6	5	4	3	2	1	0
	I2ADDR.7	I2ADDR.6	I2ADDR.5	I2ADDR.4	I2ADDR.3	I2ADDR.2	I2ADDR.1	GC

Mnemonic: I2ADDR Address: C1h

25.2.2 The Data Register, I2DAT

This register contains a byte of serial data to be transmitted or a byte which has just been received. The CPU can read from or write to this 8-bit directly addressable SFR while it is not in the process of shifting a byte. This occurs when SIO1 is in a defined state and the serial interrupt flag (SI) is set. Data in I2DAT remains stable as long as SI bit is set. While data is being shifted out, data on the bus is simultaneously being shifted in; I2DAT always contains the last data byte present on the bus. Thus, in the event of lost arbitration, the transition from master transmitter to slave receiver is made with the correct data in I2DAT.

Bit:	7	6	5	4	3	2	1	0
	I2DAT.7	I2DAT.6	I2DAT.5	I2DAT.4	I2DAT.3	I2DAT.2	I2DAT.1	I2DAT.0

Mnemonic: I2DAT Address: BCh

I2DAT and the acknowledge bit form a 9-bit shift register, the acknowledge bit is controlled by the SIO1 hardware and cannot be accessed by the CPU. Serial data is shifted through the acknowledge bit into I2DAT on the rising edges of serial clock pulses on the SCL line. When a byte has been shifted into I2DAT, the serial data is available in I2DAT, and the acknowledge bit (ACK or NACK) is returned by the control logic during the ninth clock pulse. Serial data is shifted out from I2DAT on the falling edges of SCL clock pulses, and is shifted into I2DAT on the rising edges of SCL clock pulses.

25.2.3 The Control Register, I2CON

The CPU can read from and write to this 8-bit, directly addressable SFR. Two bits are affected by the SIO1 hardware: the SI bit is set when a serial interrupt is requested, and the STO bit is cleared when a STOP condition is present on the bus. The STO bit is also cleared when ENS1 = "0".

Bit:	7	6	5	4	3	2	1	0
	-	ENS1	STA	STO	SI	AA	-	-

Mnemonic: I2CON Address: C0

BIT	NAME	FUNCTION
7	-	Reserved.
6	ENS1	0: Disable I2C Serial Function. The SDA and SCL output are in a high impedance state. SDA and SCL input signals are ignored, I2C is in the not addressed slave, and STO bit in I2CON is forced to “0”. No other bits are affected. P1.2 (SCL) and P1.3 (SDA) may be used as open drain I/O ports. 1: Enable I2C Serial Function. The P1.2 and P1.3 port latches must be to logic 1.
5	STA	The START flag. 0: The STA bit is reset, no START condition or repeated START condition will be generated. 1: The STA bit is set to enter a master mode, the I2C hardware checks the status of I2C bus and generates a START condition if the bus is free. If bus is not free, then I2C waits for a STOP condition and generates a START condition after a delay. If STA is set while I2C is already in a master mode and one or more bytes are transmitted or received, I2C transmits a repeated START condition. STA may be set any time. STA may also be set when I2C is an addressed slave.
4	STO	The bit STO bit is set while I2C is in a master mode, a STOP condition is transmitted to the I2C bus. When the STOP condition is detected on the bus, the I2C hardware clears the STO flag. In a slave mode, the STO flag may be set to recover from an bus error condition. In this cases, no STOP condition is transmitted to the I2C bus. However, the I2C hardware behaves as if a STOP condition has been received and switches to the defined not addressed slave receiver mode. The STO flag is automatically cleared by hardware. If the STA and STO bits are both set, then a STOP condition is transmitted to the I2C bus if I2C is in a master mode (in a slave mode, I2C generates an internal STOP condition which is not transmitted). I2C then transmits a START condition.
3	SI	0: When the SI flag is reset, no serial interrupt is requested, and there is no stretching on the serial clock on the SCL line. 1: When a new SIO1 state is present in the S1STATUS register, the SI flag is set by hardware, and, if the EA and ES bits (in IE register) are both set, a serial interrupt is requested. The only state that does not cause SI to be set is state F8H, which indicates that no relevant state information is available. When SI is set, the low period of the serial clock on the SCL line is stretched, and the serial transfer is suspended. A high level on the SCL line is unaffected by the serial interrupt flag. SI must be cleared by software.
2	AA	The Assert Acknowledge Flag 0: a not acknowledge (high level to SDA) will be returned during the acknowledge clock pulse on SCL when: 1) A data has been received while SIO1 is in the master receiver mode. 2) A data byte has been received while SIO1 is in the addressed slave receiver mode. 1: An Acknowledge (low level to SDA) will be returned during the acknowledge clock pulse on the SCL line when: 1) The own slave address has been received. 2) A data byte has been received while SIO1 is in the master receiver mode. 3) A data byte has been received while SIO1 is in the addressed slave receiver mode.
1	-	Reserved.
0	-	Reserved.

25.2.4 The I2C Clock Baud Rate Bits, I2CLK

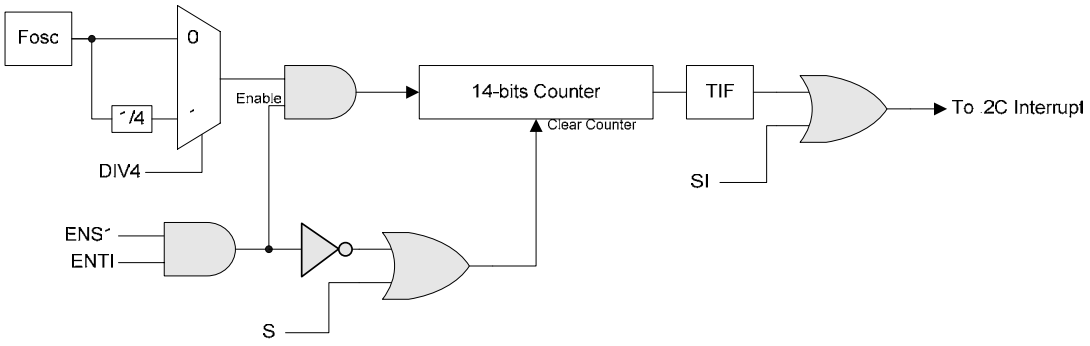
The data baud rate of I2C is determines by I2CLK register when SIO1 is in a master mode. It is not important when SIO1 is in a slave mode. In the slave modes, SIO1 will automatically synchronize with any clock frequency up to 400 KHz from master I2C device.

The data baud rate of I2C setting is Data Baud Rate of I2C = Fcpu / (I2CLK+1). The Fcpu=Fosc/4. If Fosc = 16MHz, the I2CLK = 40(28H), so data baud rate of I2C = 16MHz /(4X (40 +1)) = 97.56Kbits/sec. The block diagram is as below figure.

Bit:	7	6	5	4	3	2	1	0
	I2CLK.7	I2CLK.6	I2CLK.5	I2CLK.4	I2CLK.3	I2CLK.2	I2CLK.1	I2CLK.0

Mnemonic: I2CLK Address: BEh

BIT	NAME	FUNCTION
7 ~ 0	I2CLK	The I2C clock baud rate bits.



I2C Timer Count Block Diagram

25.2.5 The Status Register, I2STATUS

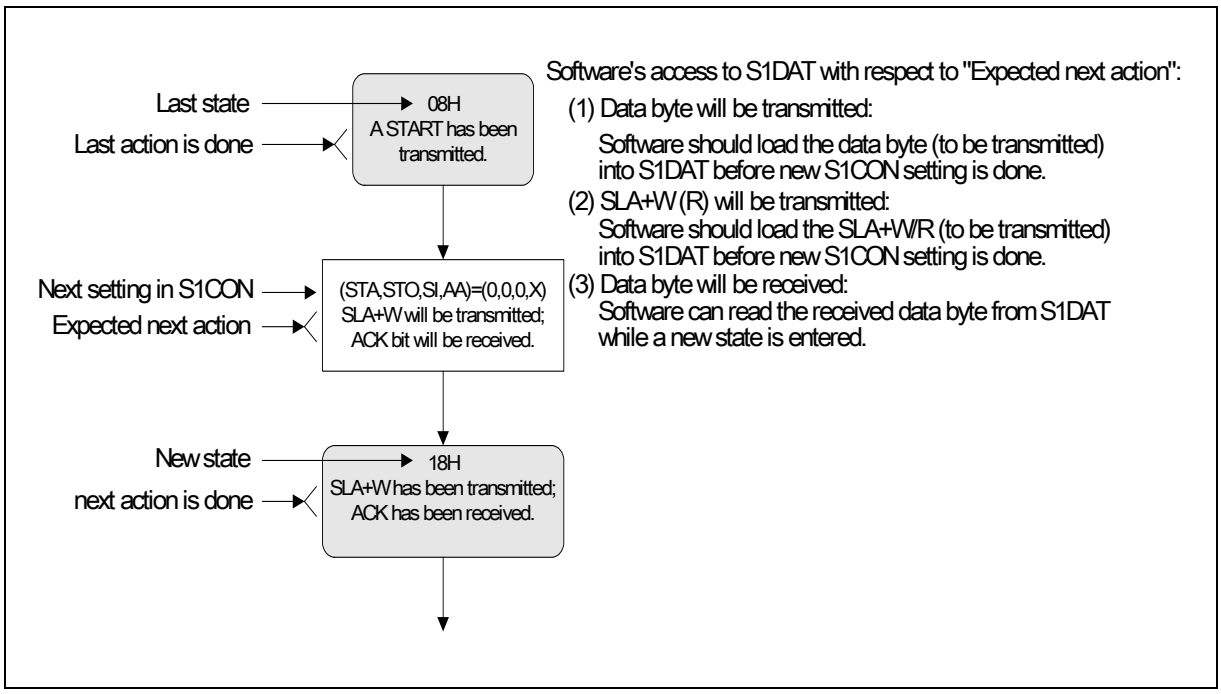
I2STATUS is an 8-bit read-only register. The three least significant bits are always 0. The five most significant bits contain the status code. There are 23 possible status codes. When I2STATUS contains F8H, no serial interrupt is requested. All other I2STATUS values correspond to defined SIO1 states. When each of these states is entered, a status interrupt is requested (SI = 1). A valid status code is present in I2STATUS one machine cycle after SI is set by hardware and is still present one machine cycle after SI has been reset by software.

In addition, state 00H stands for a Bus Error. A Bus Error occurs when a START or STOP condition is present at an illegal position in the format frame. Examples of illegal positions are during the serial transfer of an address byte, a data byte or an acknowledge bit.

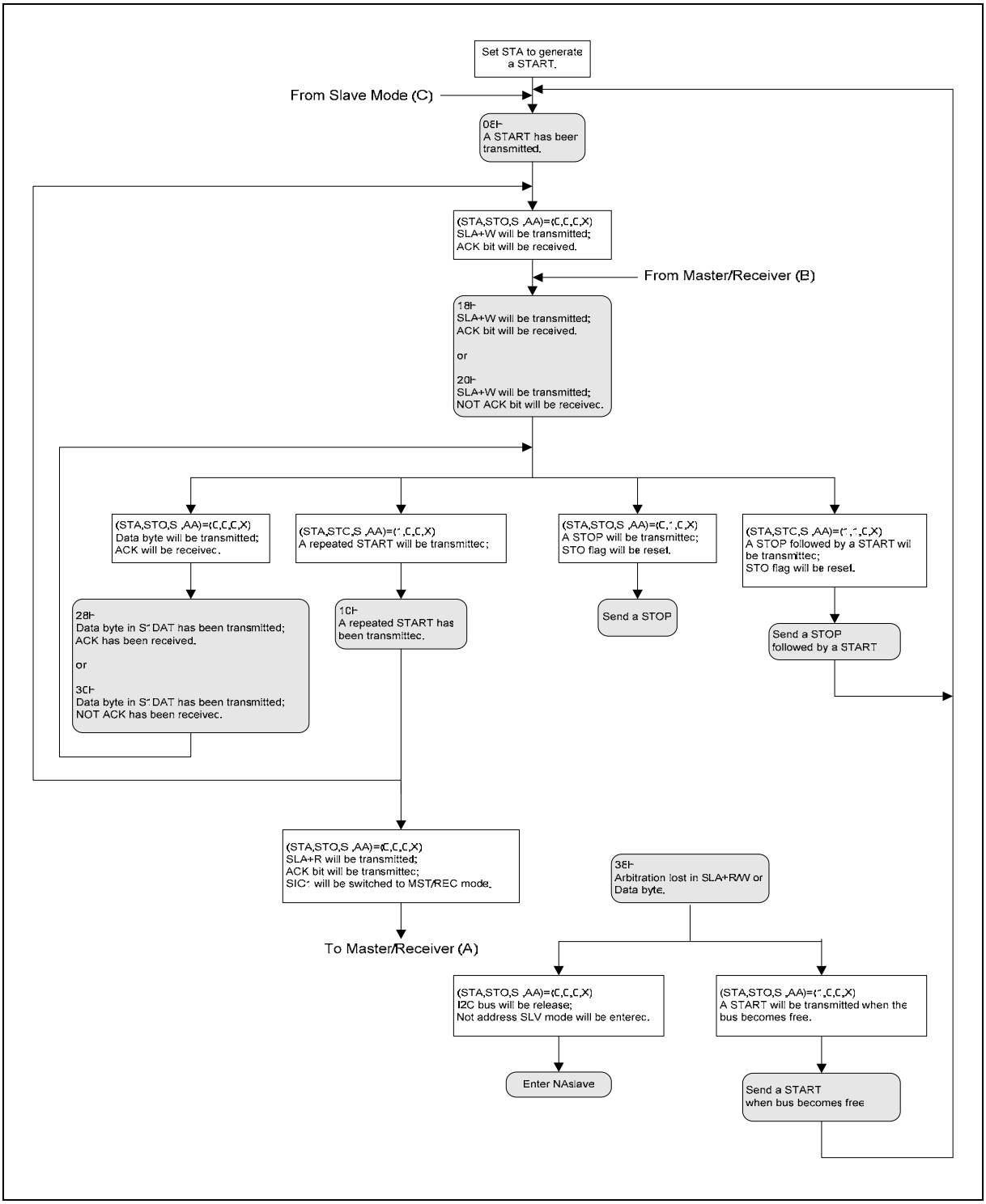
25.3 Operating Modes of I2C

The four operating modes are: Master/Transmitter, Master/Receiver, Slave/Transmitter and Slave/Receiver. Bits STA, STO and AA in I2CON decide the next action the SIO1 hardware will take after SI is cleared. When the next action is completed, a new status code in I2STATUS will be updated and SI will be set by hardware in the same time. Now, the interrupt service routine is entered (if the SI interrupt is enabled), the new status code can be used to decide which appropriate service routine the software is to branch. Data transfers in each mode are shown in the following figures.

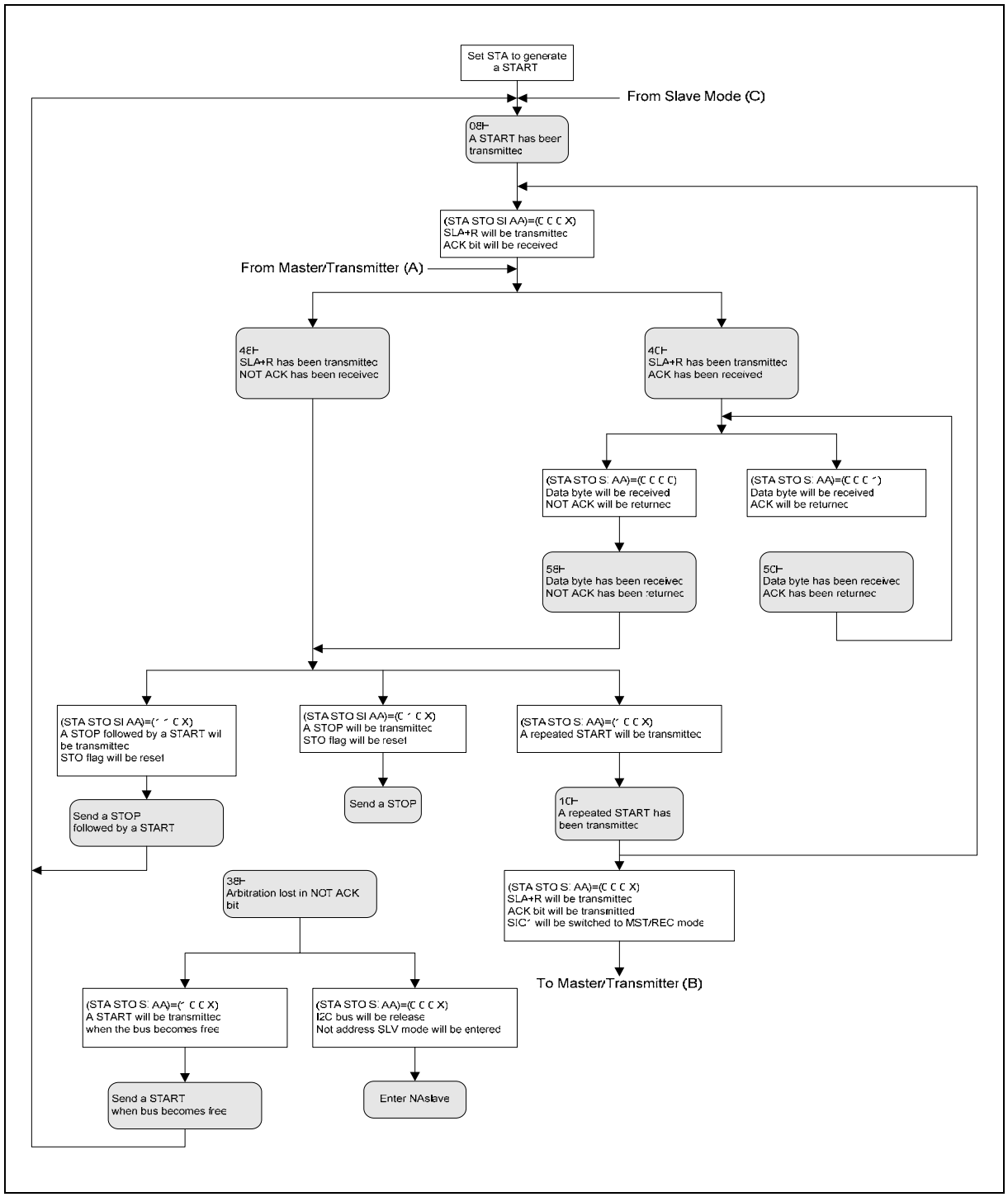
*** Legend for the following four figures:



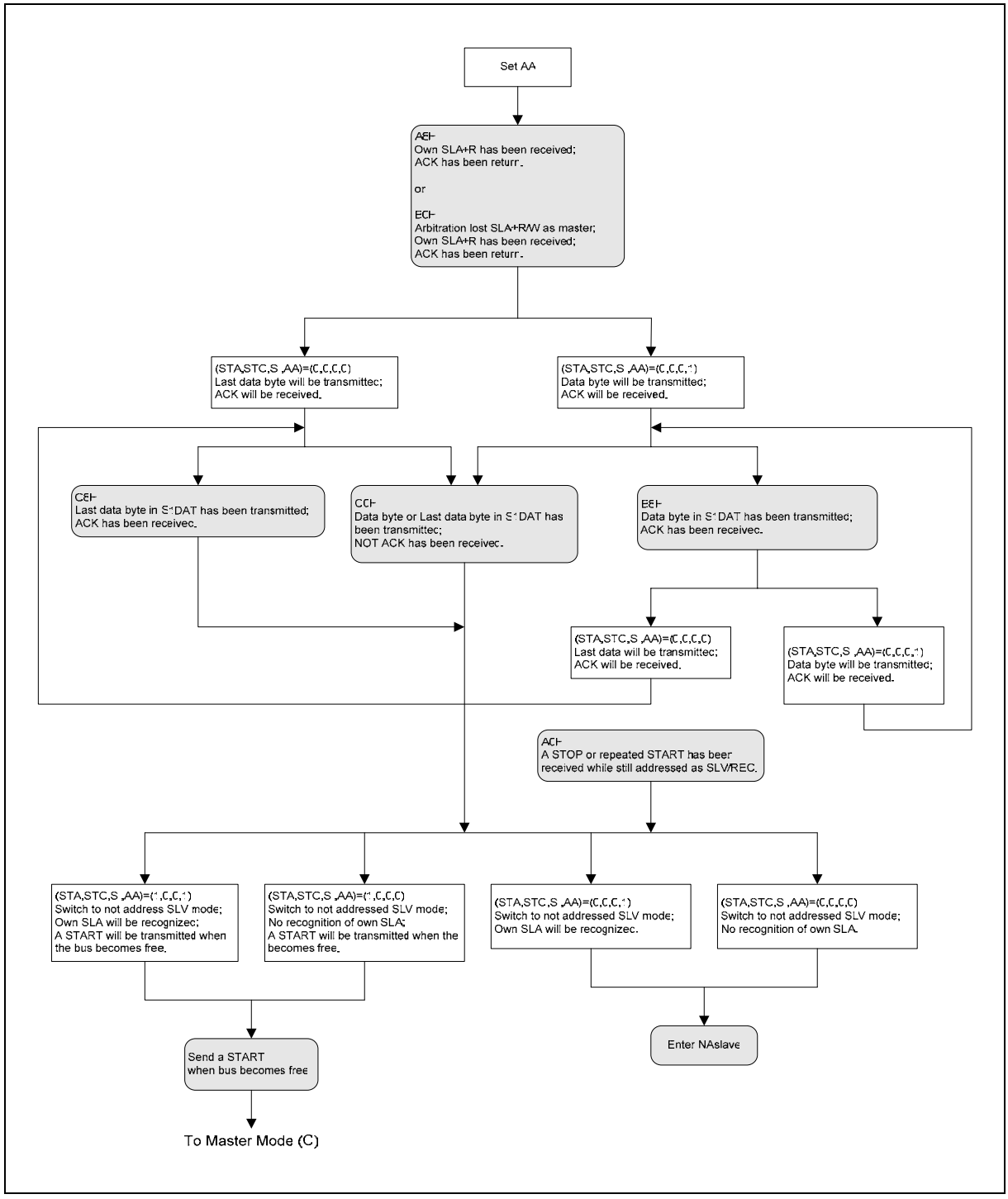
Master Transmitter Mode



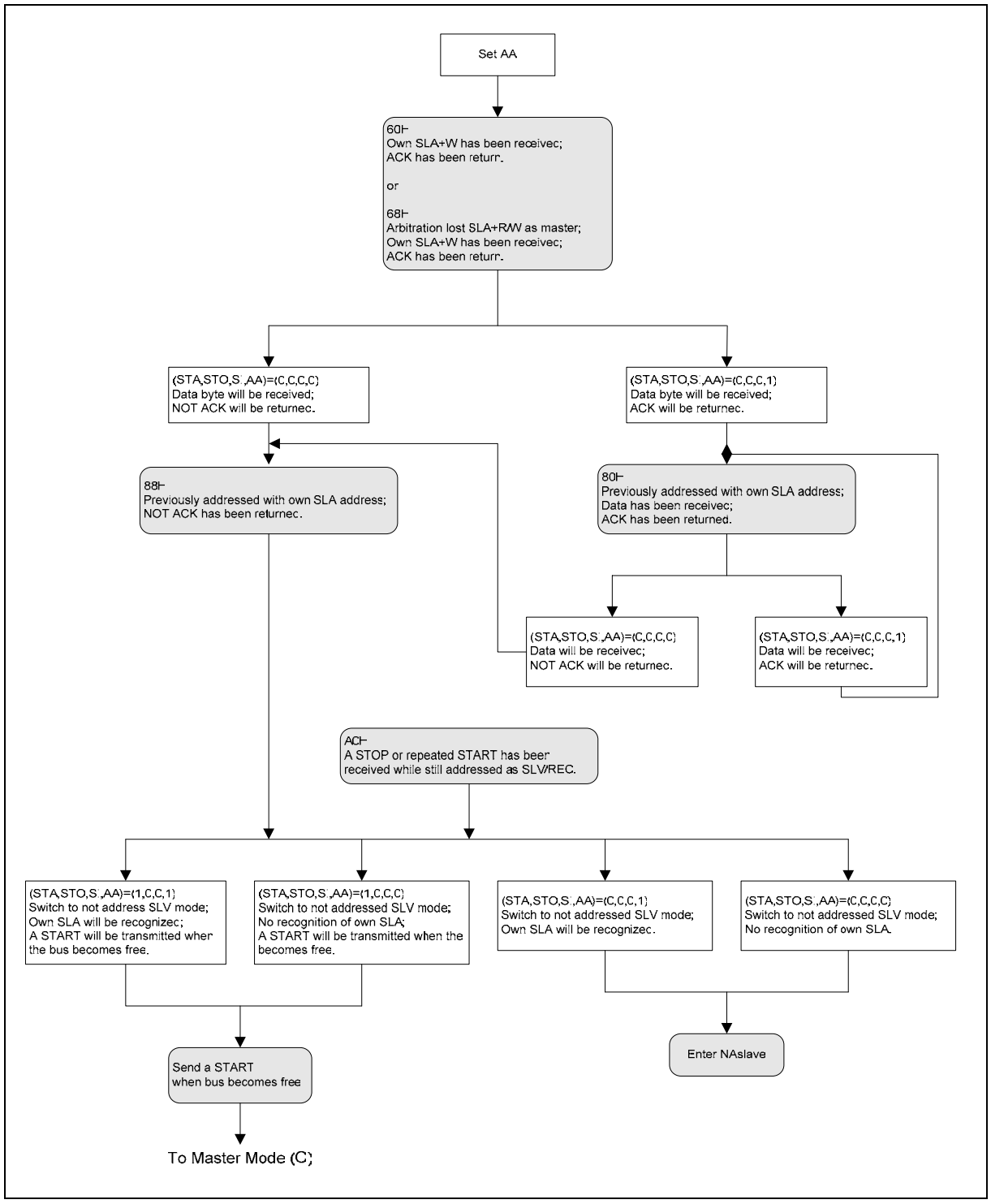
Master Receiver Mode



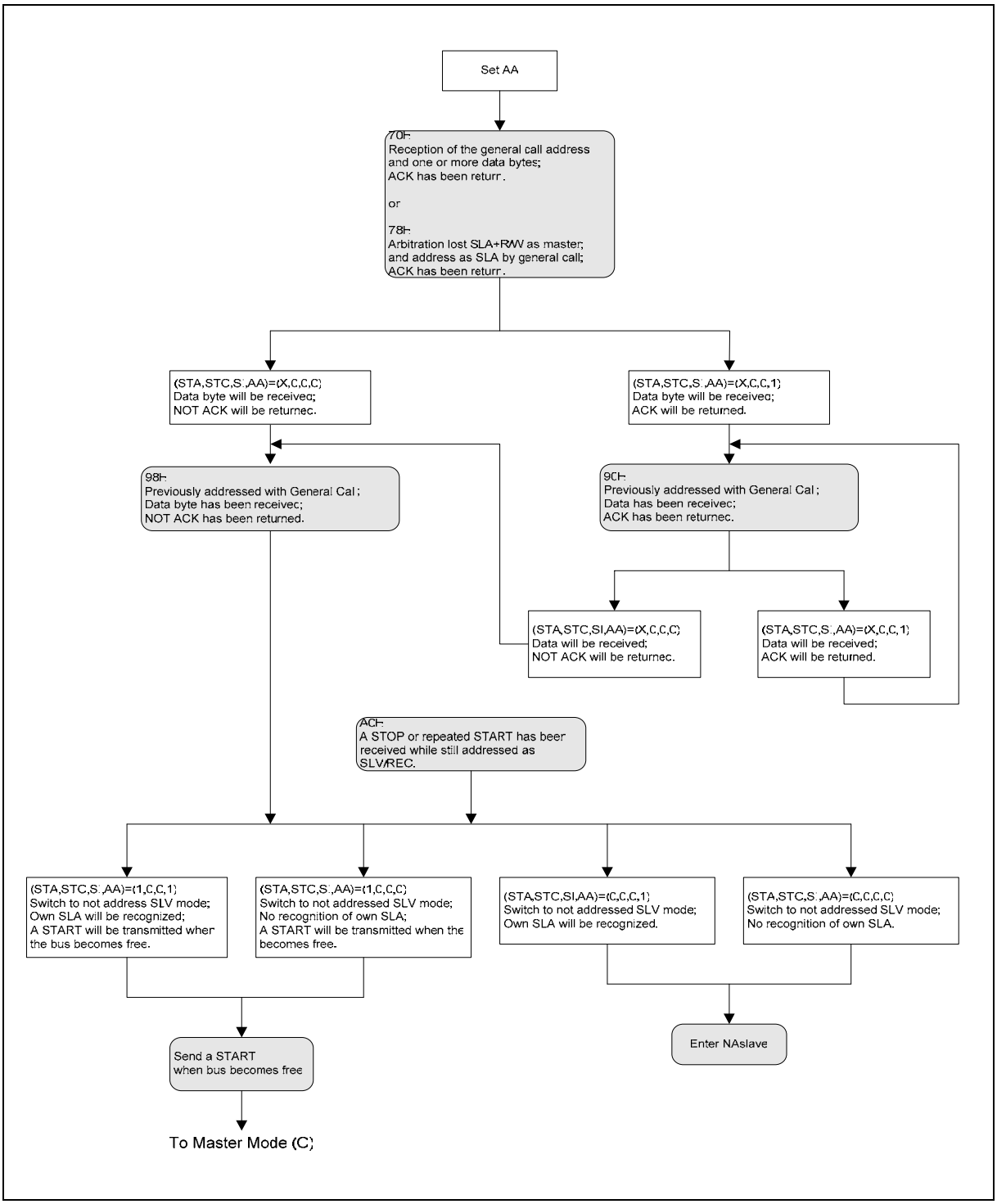
Slave Transmitter Mode



Slave Receiver Mode



GC Mode


Set AA
70H
Reception of the general call address and one or more data bytes;
ACK has been returr.
or
78H
Arbitration lost SLA+R/W as master;
and address as SLA by general call;
ACK has been returr.
(STA,STC,S:,AA)=(X,C,C,C)
Data byte will be receiveo;
NOT ACK will be returnec.
(STA,STC,S:,AA)=(X,C,C,1)
Data byte will be receiveo;
ACK will be returned.
98H
Previously addressed with General Cal;
Data byte has been receivec;
NOT ACK has been returned.
9CH
Previously addressed with General Cal;
Data has been receivec;
ACK has been returnec.
(STA,STC,SI,AA)=(X,C,C,C)
Data will be received;
NOT ACK will be returnec.
(STA,STC,S:,AA)=(X,C,C,1)
Data will be received;
ACK will be returned.
A0H
A STOP or repeated START has beer
received while still addressed as
SLV/REC.
(STA,STC,S:,AA)=(1,C,C,1)
Switch to not address SLV mode;
Own SLA will be recognized;
A START will be transmitted wher
the bus becomes free.
(STA,STC,S:,AA)=(1,C,C,C)
Switch to not addressed SLV mode;
No recognition of own SLA;
A START will be transmitted when the
becomes free.
(STA,STC,SI,AA)=(C,C,C,1)
Switch to not addressed SLV mode;
Own SLA will be recognized.
(STA,STC,S:,AA)=(C,C,C,C)
Switch to not addressed SLV mode;
No recognition of own SLA.
Send a START
when bus becomes free
Enter NAslave
To Master Mode (C)

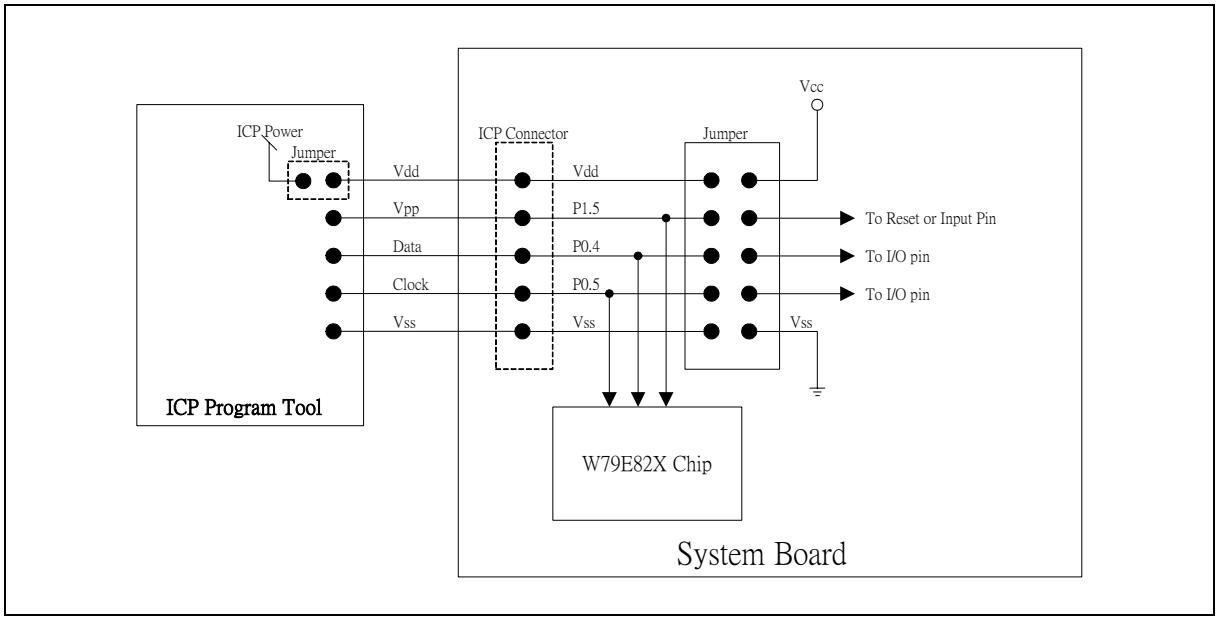
26. ICP(IN-CIRCUIT PROGRAM) FLASH PROGRAM

The contexts of flash in W79E82X series are empty by default. At the first use, you must program the flash EPROM by external Writer device or by ICP(In-Circuit Program) tool.

In the ICP tool, the user must be taken ICP's program pins before design in system design board which pins in some application circuits are P1.5, P0.4 and P0.5, as below figure. In the ICP program, the P1.5 must set to high voltage(~10.5V), and keeping this voltage to update code, data and/or configure two CONFIG bits. After finished, the high voltage of P1.5 will be released. So when use ICP program to suggest the power need power off then power on after ICP program was finished on the system board.

After entry ICP program mode, all pin will be set to quasi-bidirectional mode, and output to level "1".

The W79E82X series support program two Flash EPROM that are **16K/8K/4K/2K/1K** bytes AP Flash EPROM and **256/128** bytes NVM data memory. This mode can separate update code or all update at AP Flash EPROM or NVM data memory if need.



Note: 1. When use ICP to upgrade code, the P1.5, P0.4 and P0.5 must be taken within design system board.
2. After program finished by ICP, to suggest system power must power off and remove ICP connector then power on.

27. CONFIG BITS

The W79E82X series have two CONFIG bits(CONFIG1, CONFIG2) that must be define at power up and can not be set after the program start of execution. Those features are configured through the use of two flash EPROM bytes, and the flash EPROM can be programmed and verified repeatedly. Until the code inside the Flash EPROM is confirmed OK, the code can be protected. The protection of flash EPROM (CONFIG2) and those operations on it are described below. The data of these bytes may be read by the MOVC instruction at the addresses.

27.1 CONFIG1

CONFIG 1 :

7	6	5	4	3	2	1	0	
WDTE	RPD	PRHI	BOV	-	-	Fosc1	Fosc0	CONFIG Bit

WDTE: Watchdog Timer clock source Bit.
RPD: Reset Pin Disable Bit.
PRHI: Port Reset High or Low Bit.
BOV: Brownout voltage select Bit.
Fosc1: CPU oscillator type select Bit 1.
Fosc0: CPU oscillator type select Bit 0.

CONFIG Register 1

BIT	NAME	FUNCTION
7	WDTE	Clock source of Watchdog Timer select bit: 0: The internal RC oscillator clock is for Watchdog Timer clock used. 1: The uC clock is for Watchdog Timer clock used.
6	RPD	Reset Pin Disable bit: 0: Enable Reset function of Pin 1.5. 1: Disable Reset function of Pin 1.5, and it to be used as an input port pin.
5	PRHI	Port Reset High or Low bit: 0: Port reset to low state. 1: Port reset to high state.
4	BOV	Brownout Voltage Select bit: 0: Brownout detect voltage is 3.8V. 1: Brownout detect voltage is 2.5V.

Continued

BIT	NAME	FUNCTION
3	-	Reserved.
2	-	Reserved.
1	Fosc1	CPU Oscillator Type Select bit 1
0	Fosc0	CPU Oscillator Type Select bit 0

Oscillator Configuration bits:

FOSC1	FOSC0	OSC SOURCE
0	0	4MHz ~ 20MHz crystal
0	1	Internal RC Oscillator
1	0	Reserved
1	1	External Oscillator in XTAL1

27.2 CONFIG2

CONFIG 2 :

7	6	5	4	3	2	1	0	
C7	C6	-	-	-	-	-	-	CONFIG Bit

C7: 16K/8K/4K/2K/1K Flash EPROM Code Lock Bit.
C6: 256/128 byte Data Lock Bit.

CONFIG Register 2

C7: 16K/8K/4K/2K/1K Flash EPROM Lock bit

This bit is used to protect the customer's program code. It may be set after the programmer finishes the programming and verifies sequence. Once this bit is set to logic 0, both the Flash EPROM data and CONFIG Registers can not be accessed again.

C6: 256/128 byte Data Flash EPROM Lock bit

This bit is used to protect the customer's data code. It may be set after the programmer finishes the programming and verifies sequence. Once this bit is set to logic 0, both the data Flash EPROM and CONFIG Registers can not be accessed again.

BIT 7	BIT 6	FUNCTION DESCRIPTION
1	1	Both security of **16KB/8KB/4KB/2KB/1KB** program code and **256/128** Bytes data area are unlocked, those can be erased, programmed or read by Writer or ICP.
0	1	The **16KB/8KB/4KB/2KB/1KB** program code area is locked, it can't be read by Writer or ICP.
1	0	Don't support (Invalid)
0	0	Both security of **16KB/8KB/4KB/2KB/1KB** program code and **256/128** Bytes data area are locked, those can't be read by Writer or ICP.

28. ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	CONDITION	RATING	UNIT
DC Power Supply	VDD–VSS	-0.3	+7.0	V
Input Voltage	VIN	VSS-0.3	VDD+0.3	V
Operating Temperature	TA	-40	+85	°C
Storage Temperature	Tst	-55	+150	°C

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

29. DC ELECTRICAL CHARACTERISTICS

(TA = -40~85°C, unless otherwise specified.)

PARAMETER	SYMBOL	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operating Voltage	V_{DD}	2.7		5.5	V	V_{DD}=4.5V ~ 5.5V @ 20MHz V_{DD}=2.7V ~ 5.5V @ 12MHz
Operating Current	I_{DD}		18	25	mA	No load, RST = VSS,V_{DD}= 5.0V @ 20MHz
			6	8	mA	No load, RST = VSS, V_{DD}= 3.0V @ 12MHz
Idle Current	I_{IDLE}		11.5	15	mA	No load, V_{DD} = 5.5V @ 20MHz
			5	6.5	mA	No load, V_{DD} = 3.0V @ 12MHz
Power Down Current	I_{PWDN}		1	10	µA	No load, V_{DD} = 5.5V @ Disable BOV function
			1	10	uA	No load, V_{DD} = 3.0V @ Disable BOV function
Input Current P0, P1, P2	I_{IN1}	-50	-	+10	µA	V_{DD} = 5.5V, 0<V_{IN}<V_{DD}
Input Current RST[*1]	I_{IN2}	-55	-45	-30	µA	V_{DD} = 5.5V, V_{IN}=0.45V
Input Leakage Current P0, P1, P2 (Open Drain)	I_{LK}	-10	-	+10	µA	V_{DD} = 5.5V, 0<V_{IN}<V_{DD}
Logic 1 to 0 Transition Current P0, P1, P2	I_{TL}[*3]	-500	-	-200	µA	V_{DD} = 5.5V, VIN<2.0V
Input Low Voltage P0, P1, P2 (TTL input)	V_{IL1}	0	-	0.8	V	V_{DD} = 4.5V
		0	-	0.6	V	V_{DD} = 3.0V
Input Low Voltage XTAL1[*2]	V_{IL3}	0	-	0.8	V	V_{DD} = 4.5V
		0	-	0.4	V	V_{DD} = 3.0V
Input High Voltage XTAL1[*2]	V_{IH3}	3.5	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		2.4	-	V_{DD} +0.2	V	V_{DD} = 3.0V
Input High Voltage P0, P1, P2 (TTL input)	V_{IH1}	2.4	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		2.0	-	V_{DD} +0.2	V	V_{DD} = 3.0V
Negative going threshold (Schmitt input)	V_{ILS}	-0.5	-	0.3V_{DD}	V	
Positive going threshold (Schmitt input)	V_{IHS}	0.7V_{DD}	-	V_{DD}+0.5	V	

DC ELECTRICAL CHARACTERISTICS, continued.

PARAMETER	SYMBOL	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Hysteresis voltage	V_{HY}		$0.2V_{DD}$		V	
Source Current P0, P1, P2 (Quasi-bidirectional Mode)	I_{sr1}	-180	-210	-360	uA	V_{DD} = 4.5V, V_S = 2.4V
Sink Current P0, P1, P2 (Quasi-bidirectional Mode)	I_{SK2}	13	18.5	24	mA	V_{DD} = 4.5V, V_S = 0.45V
Output Low Voltage P0, P1, P2 (PUSH-PULL Mode)	V_{OL1}	-	0.5	0.9	V	V_{DD} = 4.5V, I_{OL} = 20 mA
		-	0.1	0.4	V	V_{DD} = 2.7V, I_{OL} = 3.2 mA
Output High Voltage P0, P1, P2 (PUSH-PULL Mode)	V_{OH}	2.4	3.4	-	V	V_{DD} = 4.5V, I_{OH} = -16mA
		1.9	2.4	-	V	V_{DD} = 2.7V, I_{OH} = -3.2mA
Brownout voltage with BOV=1	$V_{BO2.5}$	2.4	-	2.7	V	TA = -0 to 70°C
Brownout voltage with BOV=0	$V_{BO3.8}$	3.5	-	4.0	V	TA = -0 to 70°C
Comparator Reference Voltage	Vref	1.02	1.20	1.31	V	

Notes: *1. RST pin is a Schmitt trigger input.

*2. XTAL1 is a CMOS input.

*3. Pins of P0, P1,P2 can source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when Vin approximates to 2V.

29.1 The ADC Converter DC ELECTRICAL CHARACTERISTICS

(V_{DD}–V_{SS} = 3.0~5V, TA = -40~85°C, Fosc = 20MHz, unless otherwise specified.)

PARAMETER	SYMBOL	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Analog input	AVIN	V_{SS}-0.2		V_{DD}+0.2	V	
ADC clock	ADCCLK	200KHz		5MHz	Hz	ADC circuit input clock
Conversion time	t_C		$52t_{ADC}$[1]		us	
Differential non-linearity	DNL	-1	-	+1	LSB	
Integral non-linearity	INL	-2	-	+2	LSB	
Offset error	Ofe	-1	-	+1	LSB	
Gain error	Ge	-1	-	+1	%	
Absolute voltage error	Ae	-3	-	+3	LSB	

Notes:

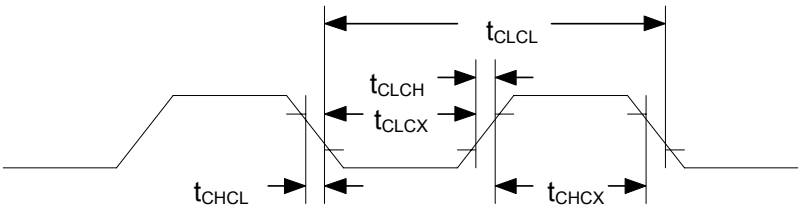
1. tADC: The period time of ADC input clock.

29.2 The COMPARATOR ELECTRICAL CHARACTERISTICS

(V_{DD}–V_{SS} = 3.0~5V, TA = -40~85°C, Fosc = 20MHz, unless otherwise specified.)

PARAMETER	SYMBOL	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Common mode range comparator inputs	V_{CR}	0		V_{DD}-0.3	V	
Common mode rejection ratio	CMRR			-50	dB	
Response time	t_{RS}	-	30	100	ns	
Comparator enable to output valid time	t_{EN}	-	1	5	us	
Input leakage current, comparator	I_{IL}	-10	0	10	uA	0< V_{IN} <V_{DD}

30. AC ELECTRICAL CHARACTERISTICS



Note: Duty cycle is 50%.

31. EXTERNAL CLOCK CHARACTERISTICS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Clock High Time	t_{CHCX}	12.5	-	-	nS	
Clock Low Time	t_{CLCX}	12.5	-	-	nS	
Clock Rise Time	t_{CLCH}	-	-	10	nS	
Clock Fall Time	t_{CHCL}	-	-	10	nS	

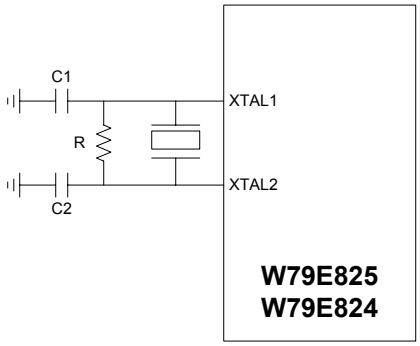
32. AC SPECIFICATION

PARAMETER	SYMBOL	VARIABLE CLOCK MIN.	VARIABLE CLOCK MAX.	UNITS
Oscillator Frequency	$1/t_{CLCL}$	0	20	MHz

33. TYPICAL APPLICATION CIRCUITS

CRYSTAL	C1	C2	R
4MHz ~ 20 MHz	without	without	without

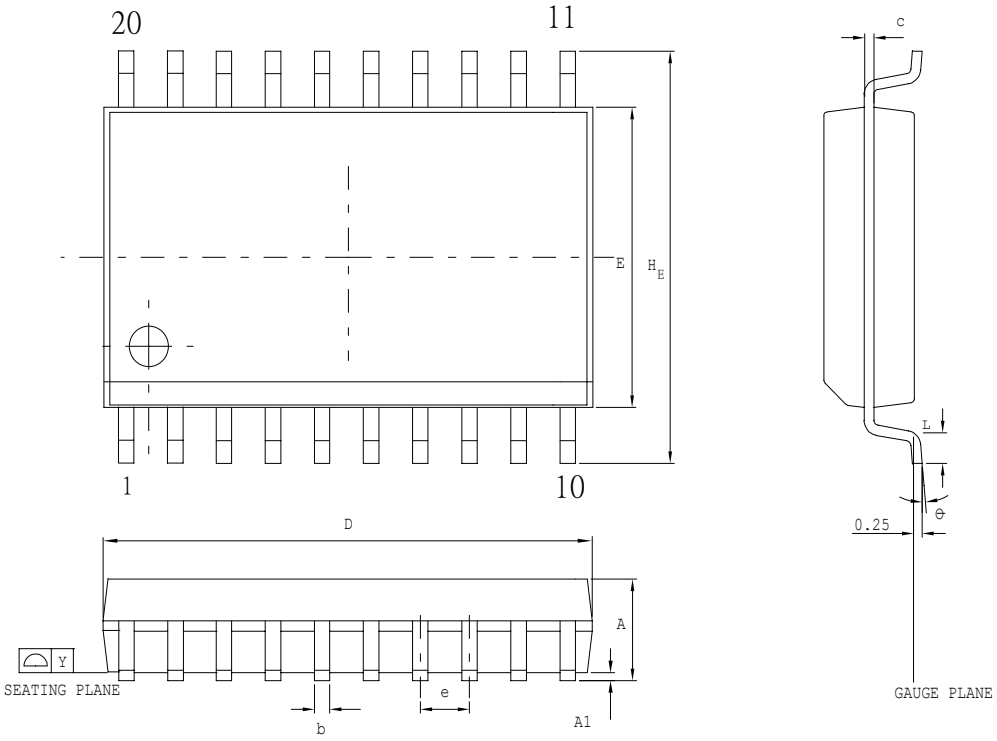
The above table shows the reference values for crystal applications.



34. PACKAGE DIMENSIONS

34.1 20-pin SO

20L SOP-300mil

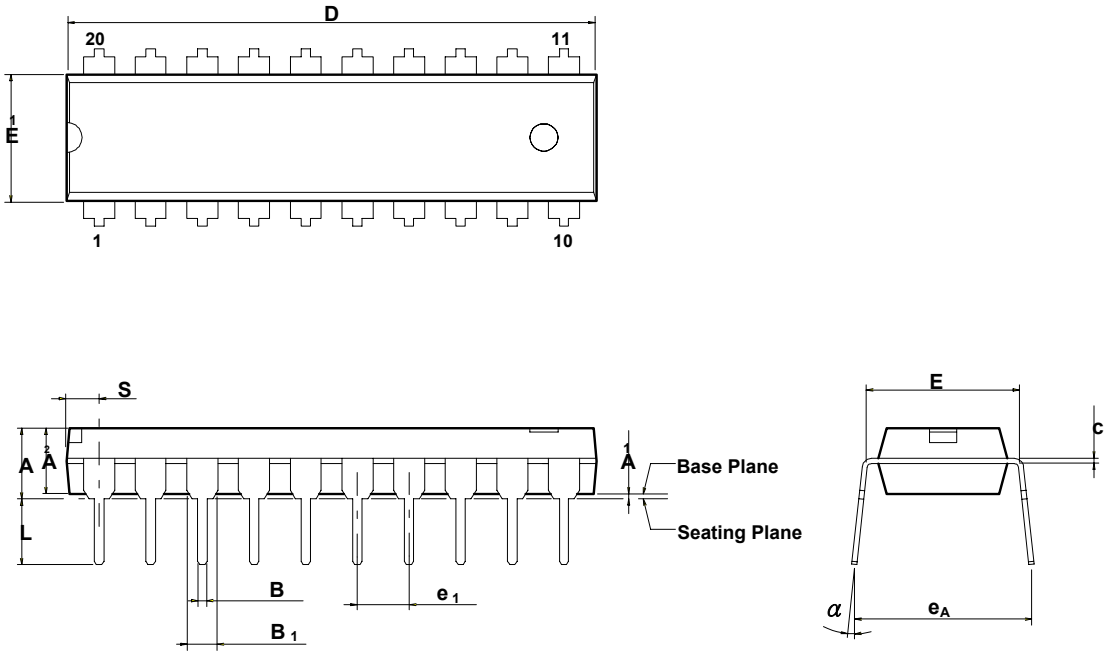


Control demensions are in milmeters .

SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	MAX.	MIN.	MAX.
A	2.35	2.65	0.093	0.104
A1	0.10	0.30	0.004	0.012
b	0.33	0.51	0.013	0.020
c	0.23	0.32	0.009	0.013
E	7.40	7.60	0.291	0.299
D	12.60	13.00	0.496	0.512
e	1.27 BSC		0.050 BSC	
H_E	10.00	10.65	0.394	0.419
Y	—	0.10	—	0.004
L	0.40	1.27	0.016	0.050
θ	0	8	0	8

34.2 20-pin DIP

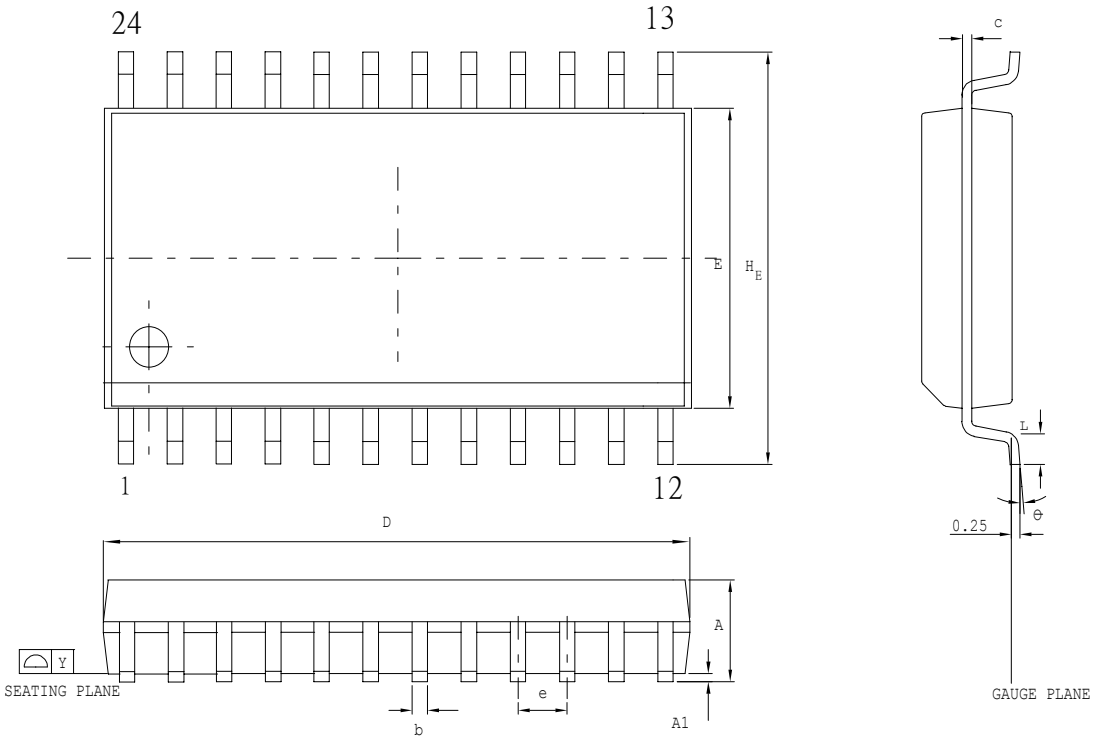
20L PDIP 300mil



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.175	—	—	4.45
A_1	0.010	—	—	0.25	—	—
A_2	0.125	0.130	0.135	3.18	3.30	3.43
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.058	0.060	0.064	1.47	1.52	1.63
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	1.026	1.040	—	20.06	26.42
E	0.290	0.300	0.310	7.37	7.62	7.87
E_1	0.245	0.250	0.255	6.22	6.35	6.48
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
α	0	—	15	0	—	15
e_A	0.335	0.355	0.375	8.51	9.02	9.53
S	—	—	0.075	—	—	1.91

34.3 24-pin SO

24L SOP-300mil



Control demensions are in milmeters .

SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	MAX.	MIN.	MAX.
A	2.35	2.65	0.093	0.104
A1	0.10	0.30	0.004	0.012
b	0.33	0.51	0.013	0.020
c	0.23	0.32	0.009	0.013
E	7.40	7.60	0.291	0.299
D	15.20	15.60	0.598	0.614
e	1.27 BSC		0.050 BSC	
H_E	10.00	10.65	0.394	0.419
Y	—	0.10	—	0.004
L	0.40	1.27	0.016	0.050
θ	0	8	0	8

35. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Mar. 30, 2006	-	Initial Issued
A2	June 04, 2006		To add W79E823/822/821 parts and function description
A3	June 19, 2006	4~5	To remove normal package of part number list
A4	June 23, 2006	86~92	To revise PWM function of W79E823, W79E822 and W79E821 to 4 PWM output channel
A5	Nov. 27, 2006	8 94 108~109 96 89	1. To remove block diagram. 2. To add GC call function description. 3. Revise DC characteristics spec. 4. Revise Timer Counter of I2C block diagram. 5. Revise “Release brake of PWM” flow chart.

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